



L6132

LINEAR INTEGRATED CIRCUIT

GENERAL PURPOSE, LOW VOLTAGE, RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

DESCRIPTION

The UTC **L6132** is a dual op amp with low supply current and low voltage (2.7-5.5V). It brings nice performance to low voltage and low power systems. With a 1MHz unity-gain frequency. The UTC **L6132** has a guaranteed 1 V/ μ s slew rate and low supply current. It provides heavy rail-to-rail (R-to-R) output swing loads and the input common-mode voltage range including ground. Besides, it is also capable for comfortably driving large capacitive loads.

The UTC **L6132** has bipolar input and CMOS output for improved noise performance and higher output current drive. It's the most cost effective solution for the applications where low voltage operation, space saving and low price are required.

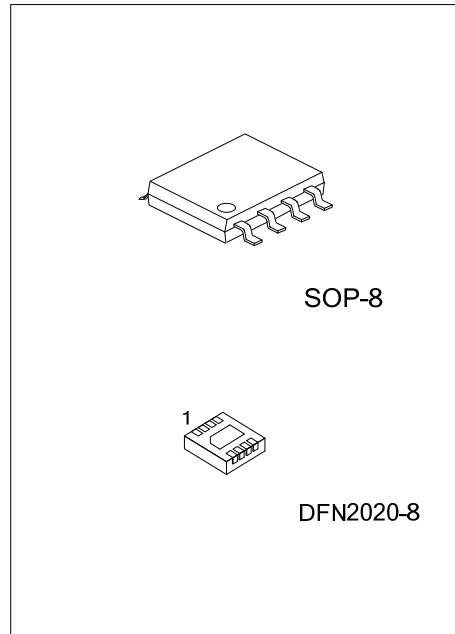
FEATURES

- * 2.7V and 5V Performance Guaranteed
- * No Crossover Distortion
- * 210 μ A Low Supply Current
- * Rail-to-Rail Output Swing
@10k Ω Load V^+ -10mV
 V^- +65mV
- * V_{CM} From -0.2V to V^+ -0.8V

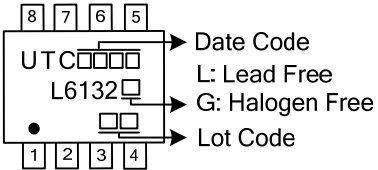
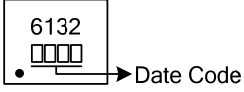
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
L6132L-S08-R	L6132G-S08-R	SOP-8	Tape Reel
L6132L-K08-2020-R	L6132G-K08-2020-R	DFN2020-8	Tape Reel

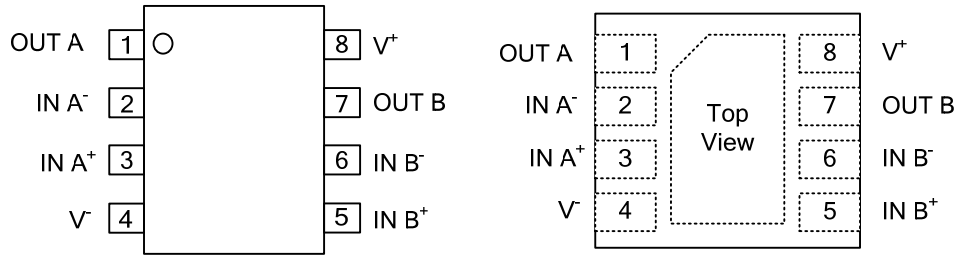
<p>L6132G-S08-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S08: SOP-8, K08-2020: DFN-8(2x2)</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

SOP-8	DFN2020-8
 <p>The diagram shows an SOP-8 package with markings: 'UTC' and 'L6132' in the center, a date code '8765' at the top, and a lot code '1234' at the bottom. A dot is located on the left side. Arrows point from the date code, 'L6132', and lot code to their respective labels: 'Date Code', 'L: Lead Free', 'G: Halogen Free', and 'Lot Code'.</p>	 <p>The diagram shows a DFN2020-8 package with markings: '6132' and a date code '8765' in the center, and a dot on the left side. An arrow points from the date code to the label 'Date Code'.</p>

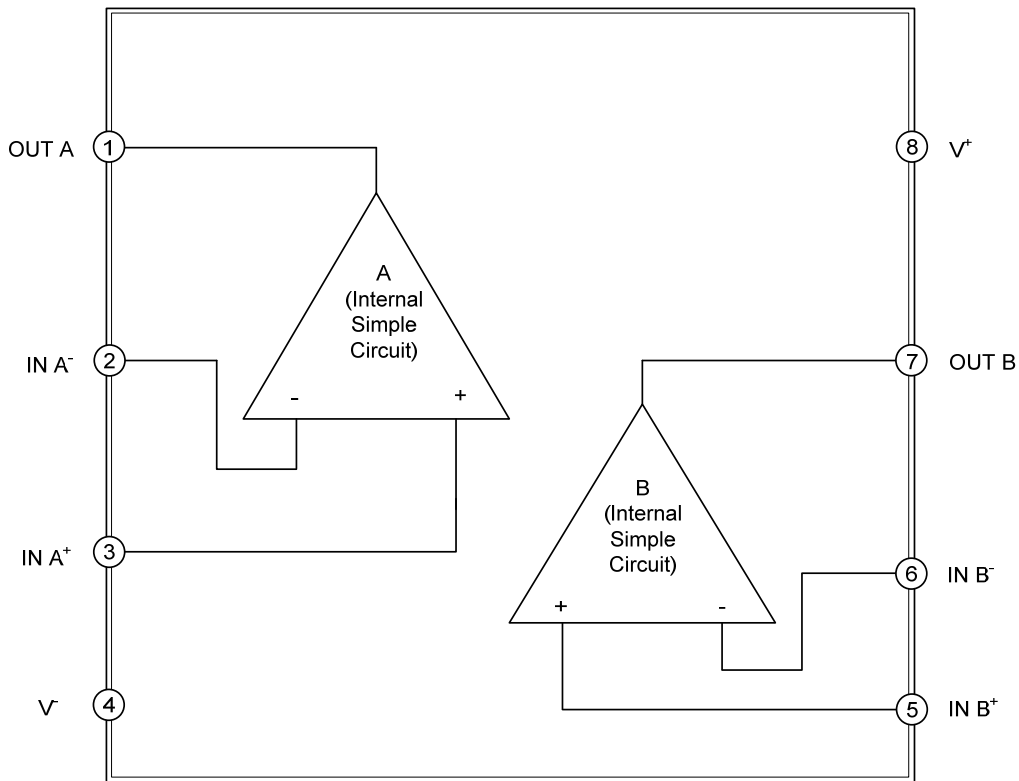
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	OUTA	Output for Channel 1
2	IN A ⁻	Negative Input for Channel 1
3	IN A ⁺	Positive Input for Channel 1
4	V ⁻	Supply Output Voltage
5	IN B ⁺	Positive Input for Channel 2
6	IN B ⁻	Negative Input for Channel 2
7	OUT B	Output for Channel 2
8	V ⁺	Supply Input Voltage

BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Note1)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{SS}	2.7~5.5	V
Supply Voltage (V^+ - V^-)		V_{SS}	5.5	V
Differential Input Voltage		$V_{I(DIFF)}$	±Supply Voltage	
Output Short Circuit	V^+	$I_{O(SC)}$	(Note 2)	
	V^-		(Note 3)	
Infrared (15 sec)			215	°C
Junction Temperature		T_J	+150	°C
Operation Temperature		T_{OPR}	-40~+85	°C
Storage Temperature		T_{STG}	-65~+150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- Shorting output to V^+ will adversely affect reliability
- Shorting output to V^- will adversely affect reliability

■ THERMAL INFORMATION (Note)

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ_{JA}	250	°C/W
	DFN2020-8		155	°C/W
Junction to Case	SOP-8	θ_{JC}	140	°C/W
	DFN2020-8		20	°C/W

Note: θ_{JA} is measured in the natural convection at $T_A=25^\circ\text{C}$ on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

■ ELECTRICAL CHARACTERISTICS (FOR 2.7V)

All limits guaranteed for $T_J=25^\circ\text{C}$, $V^+=2.7\text{V}$, $V^-=0\text{V}$, $V_{CM}=1.0\text{V}$, $V_{OUT}=V^+/2$ and $R_L>1\text{M}\Omega$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
Input Offset Voltage	V_{OS}			1.7	6	mV
Input Common Mode Voltage Range	V_{CM}	For $\text{CMRR}\geq 50\text{dB}$	0	-0.2		V
				1.9	1.7	V
Output Swing	V_{OUT}	$R_L=10\text{k}\Omega$ to 1.35V	V^+-100	V^+-10		mV
				60	180	mV
Input Offset Voltage Average Drift	TCV_{OS}			5		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_{I(BIAS)}$			11	250	nA
Input Offset Current	$I_{I(OFF)}$			5	50	nA
Common Mode Rejection Ratio	CMRR	$0\text{V}\leq V_{CM}\leq 1.7\text{V}$	50	63		dB
Power Supply Rejection Ratio	PSRR	$2.7\text{V}\leq V^+\leq 5\text{V}$, $V_{OUT}=1\text{V}$	50	60		dB
Supply Current	I_{SS}	Both amplifiers		140	340	μA
AC CHARACTERISTICS						
Gain Bandwidth Product	GBWP	$C_L=200\text{pF}$		1		MHz
Phase Margin	Φ_m			60		Deg
Gain Margin	G_m			10		dB
Input Referred Voltage Noise	eN	F=1KHz		46		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
Input Referred Current Noise	i_n	F=1KHz		0.17		$\frac{\text{pA}}{\sqrt{\text{Hz}}}$

■ ELECTRICAL CHARACTERISTICS (FOR 5V)

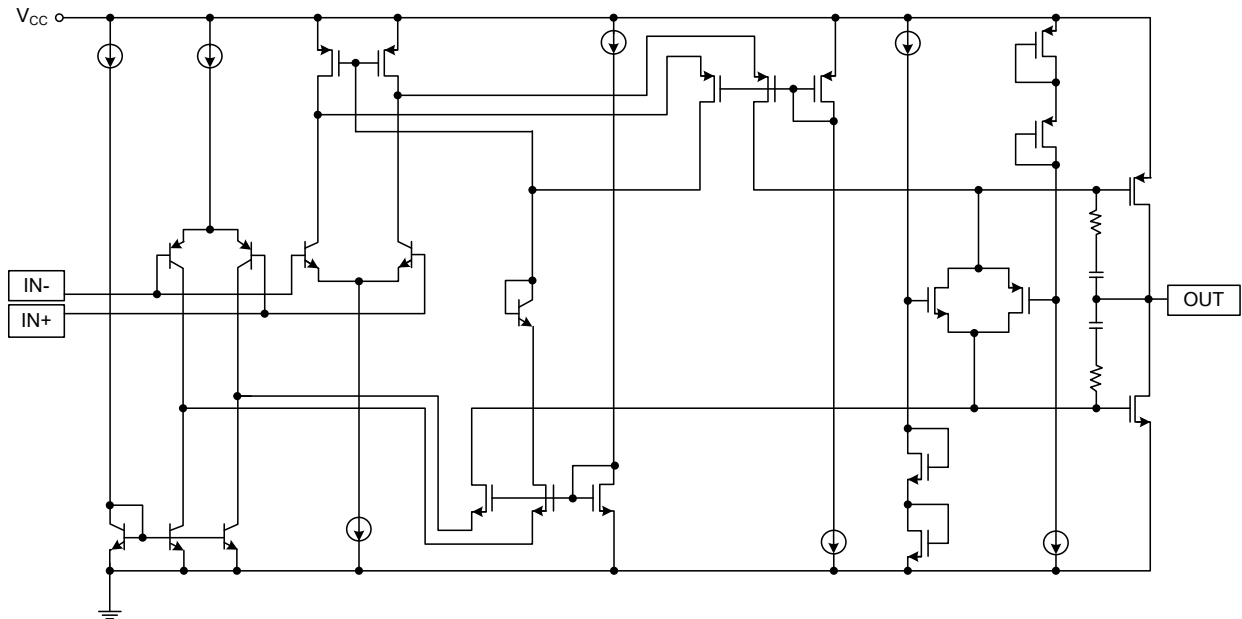
All limits guaranteed for $T_J=25^{\circ}\text{C}$, $V^+=5\text{V}$, $V^-=0\text{V}$, $V_{\text{CM}}=2.0\text{V}$, $V_{\text{OUT}}=V^+/2$ and $R_L > 1\text{M}\Omega$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	
DC CHARACTERISTICS							
Input Offset Voltage	V_{OS}			1.7	6	mV	
Input Common-Mode Voltage Range	V_{CM}	For $\text{CMRR} \geq 50\text{dB}$	0	-0.2		V	
				4.2	4	V	
Output Swing	V_{OUT}	$R_L=2\text{K}\Omega$ to 2.5V	V_{OH}	V^+-300	V^+-40	mV	
			V_{OL}		120	300	mV
		$R_L=10\text{K}\Omega$ to 2.5V	V_{OH}	V^+-100	V^+-10		mV
			V_{OL}		65	180	mV
Input Offset Voltage Average Drift	TCVos			5		$\mu\text{V}/^{\circ}\text{C}$	
Input Bias Current	$I_{\text{(BIAS)}}$			15	250	nA	
Input Offset Current	$I_{\text{(OFF)}}$			5	50	nA	
Common Mode Rejection Ratio	CMRR	$0\text{V} \leq V_{\text{CM}} \leq 4\text{V}$	50	65		dB	
Power Supply Rejection Ratio	PSRR	$2.7\text{V} \leq V^+ \leq 5\text{V}$ $V_{\text{OUT}}=1\text{V}$, $V_{\text{CM}}=1\text{V}$	50	60		dB	
Large Signal Voltage Gain (Note 1)	G_V	$R_L=2\text{K}\Omega$	15	100		V/mV	
Output Short Circuit Current	I_{OUT}	Sourcing, $V_{\text{OUT}}=0\text{V}$	10	230		mA	
		Sinking, $V_{\text{OUT}}=5\text{V}$	30	160		mA	
Supply Current	I_{SS}	Both Amplifiers		210	440	μA	
AC CHARACTERISTICS							
Slew Rate	SR	(Note 2)		1		$\text{V}/\mu\text{s}$	
Gain Bandwidth Product	GBWP	$C_L=200\text{pF}$		1		MHz	
Phase Margin	Φ_m			60		Deg	
Gain Margin	G_m			10		dB	
Input Referred Voltage Noise	eN	$f=1\text{KHz}$		39		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	
Input Referred Current Noise	i_n	$f=1\text{KHz}$		0.21		$\frac{\text{pA}}{\sqrt{\text{Hz}}}$	

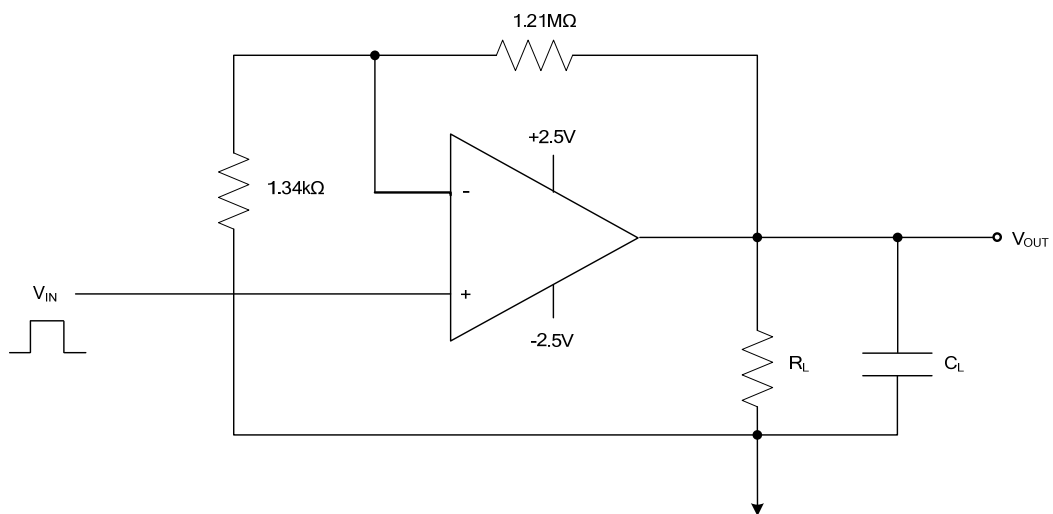
Notes: 1. R_L is connected to V^- . The output voltage is $0.5\text{V} \leq V_{\text{OUT}} \leq 4.5\text{V}$.

2. Connected as voltage follower with 3V step input. Number specified is these lower of the positive and negative slew rates

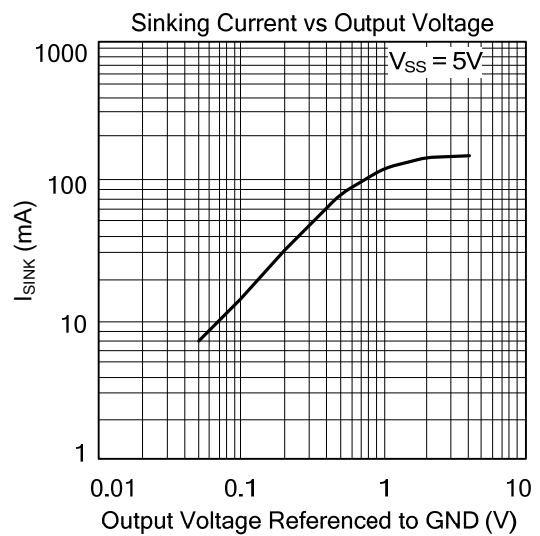
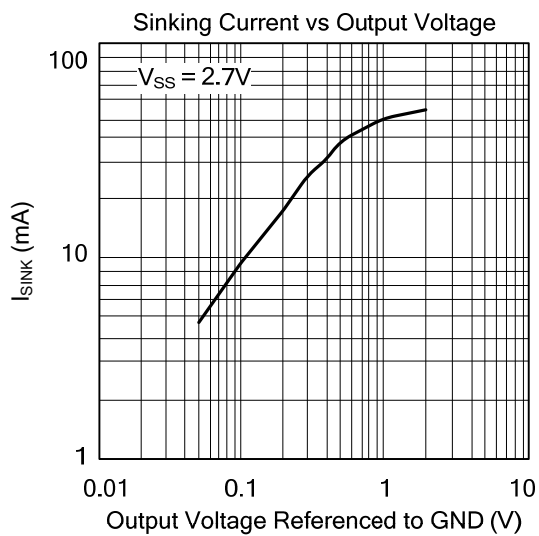
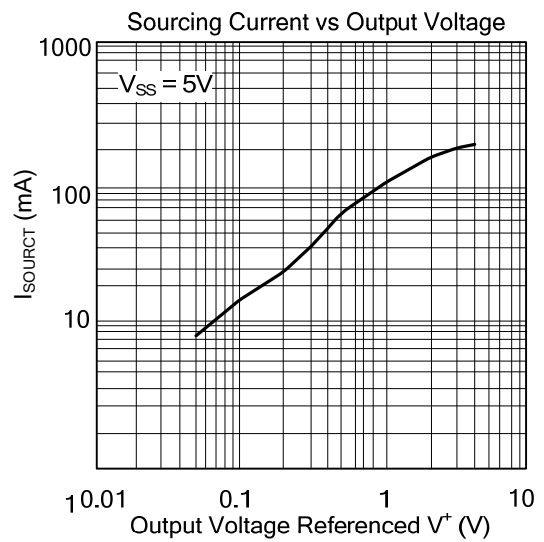
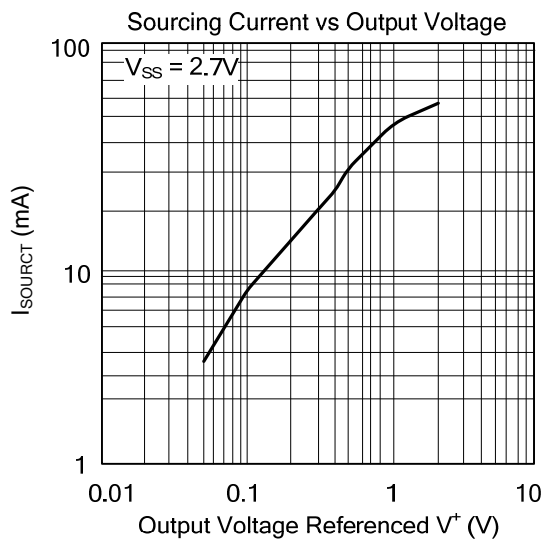
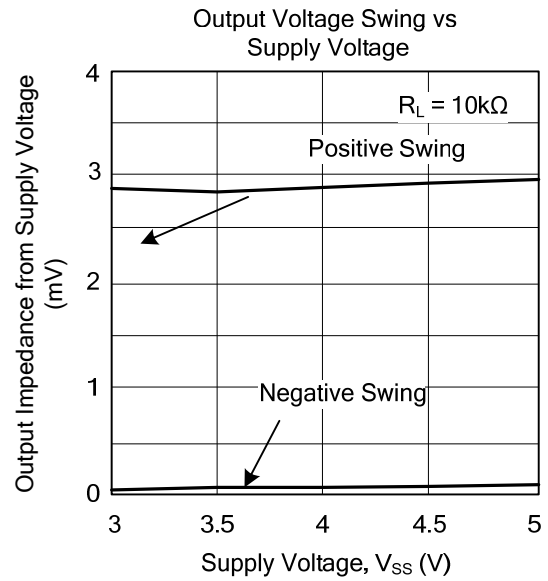
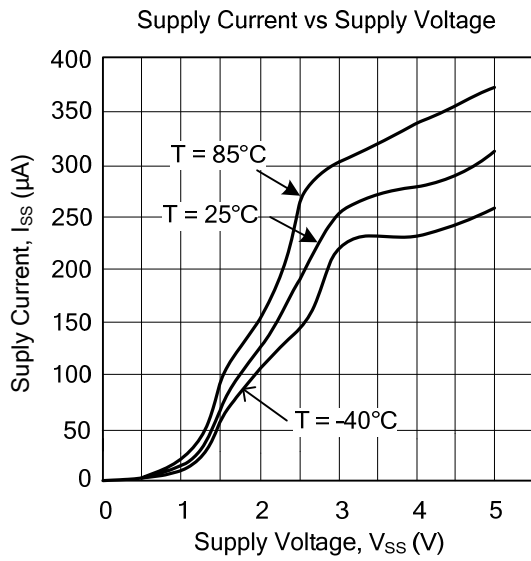
INTERNAL SIMPLE CIRCUIT



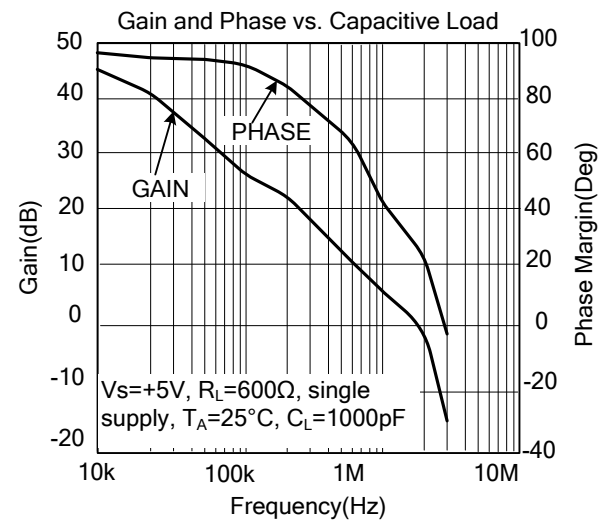
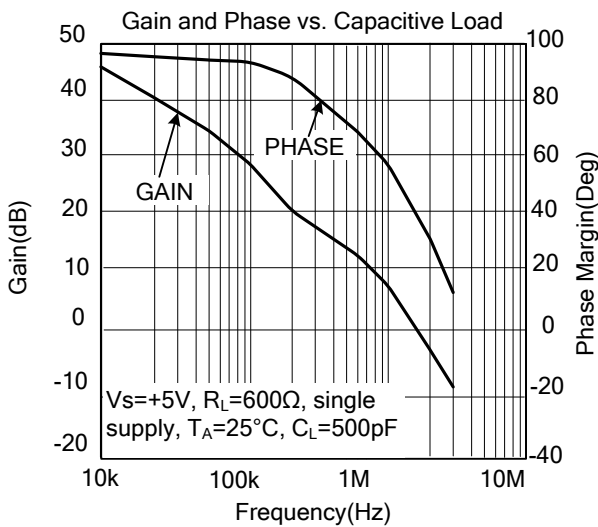
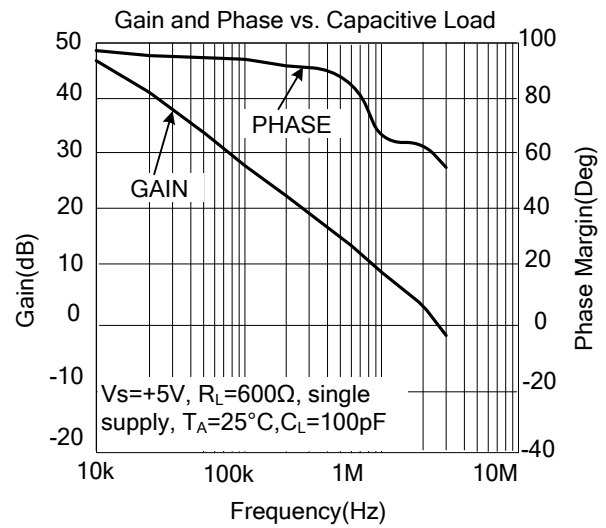
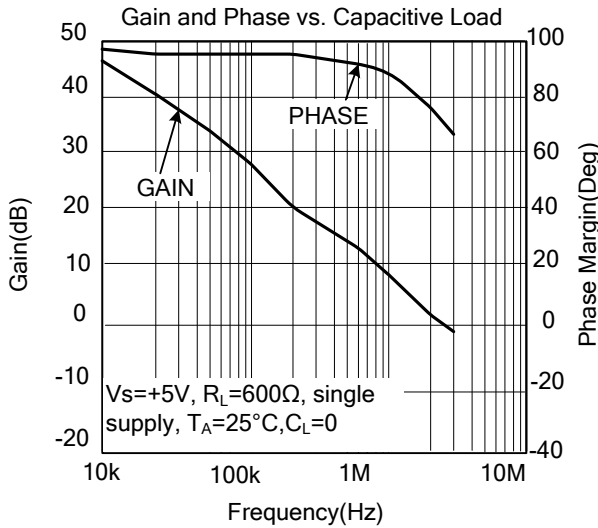
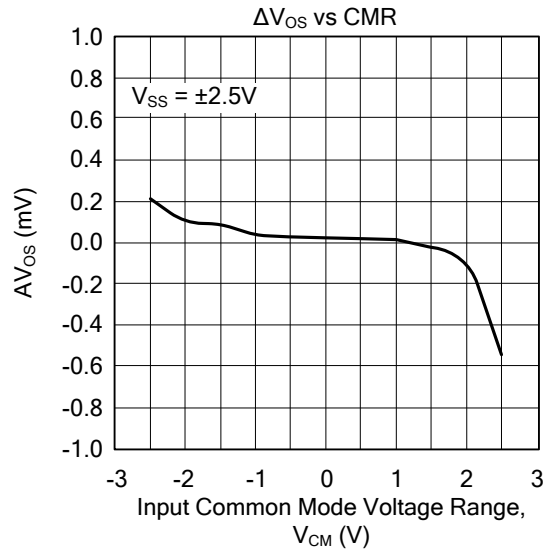
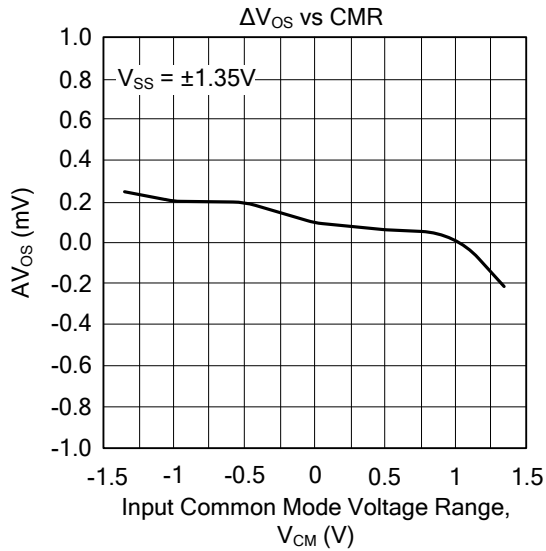
TEST CIRCUIT FOR STABILITY VS CAPACITIVE LOAD



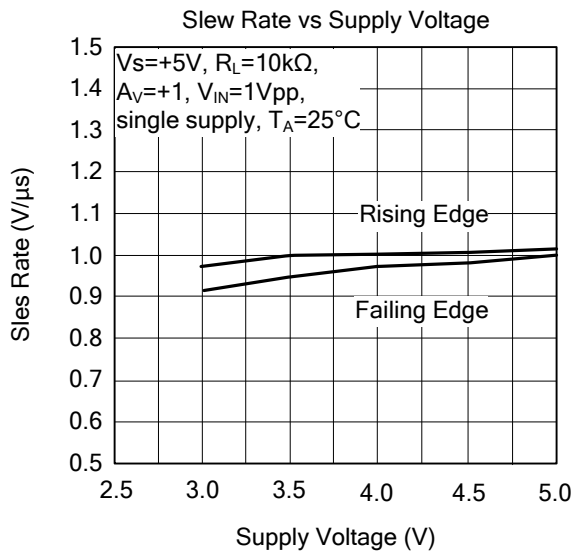
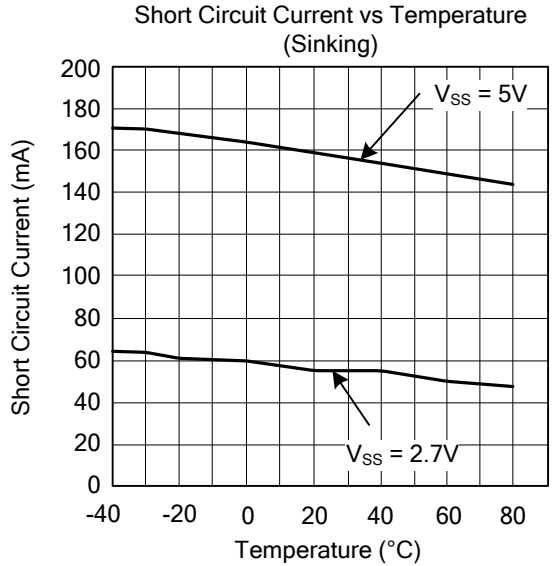
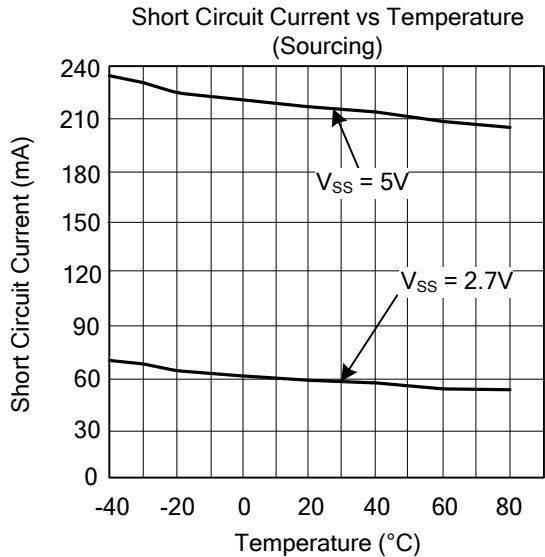
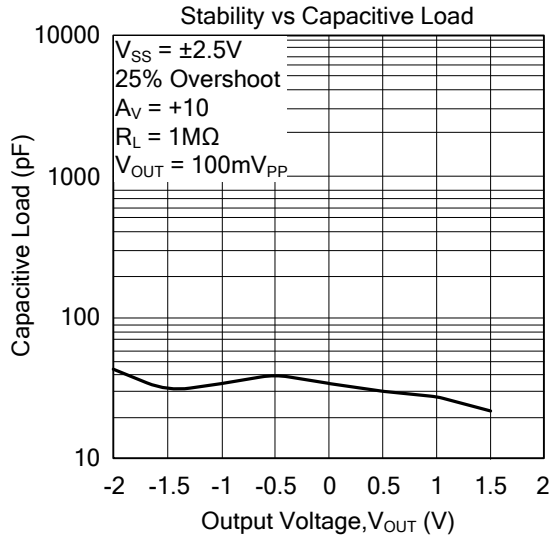
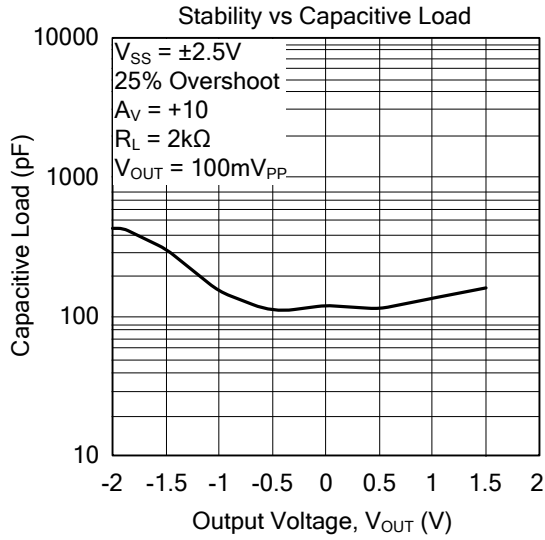
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS(Cont.)

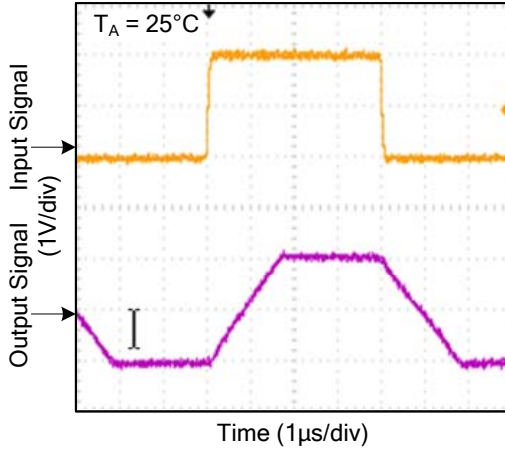


■ TYPICAL CHARACTERISTICS(Cont.)

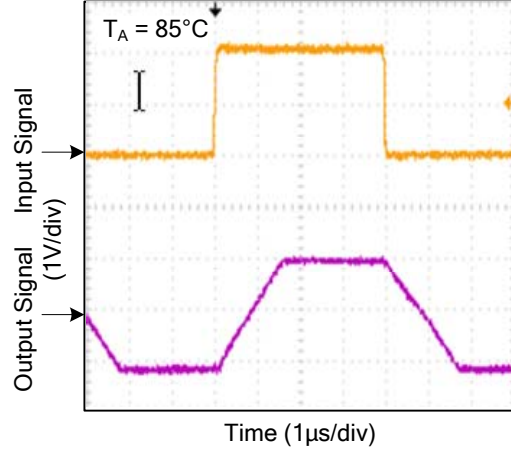


■ TYPICAL CHARACTERISTICS(Cont.)

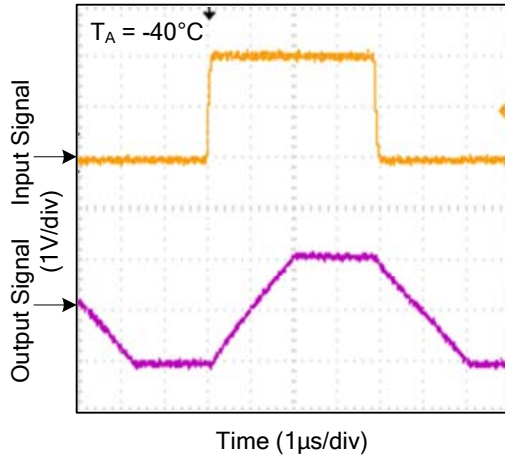
Non-Inverting Large Signal Pulse Response



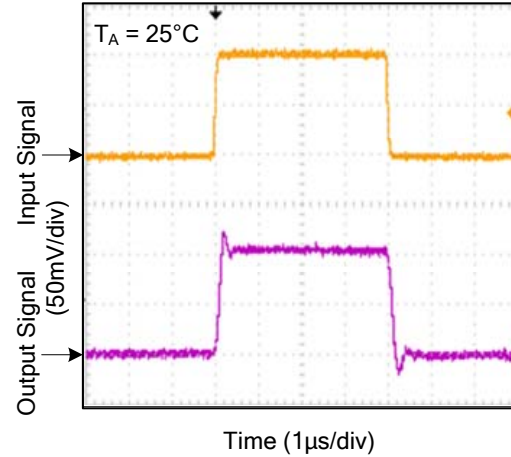
Non-Inverting Large Signal Pulse Response



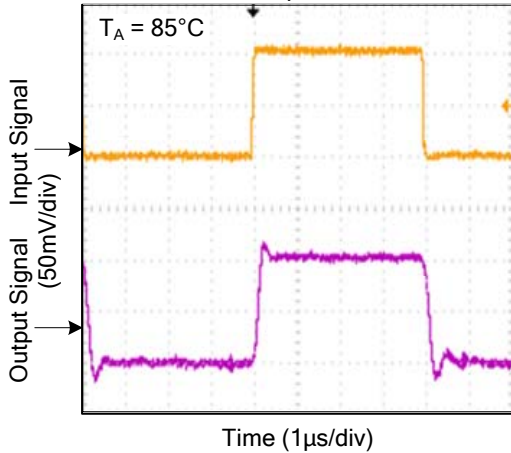
Non-Inverting Large Signal Pulse Response



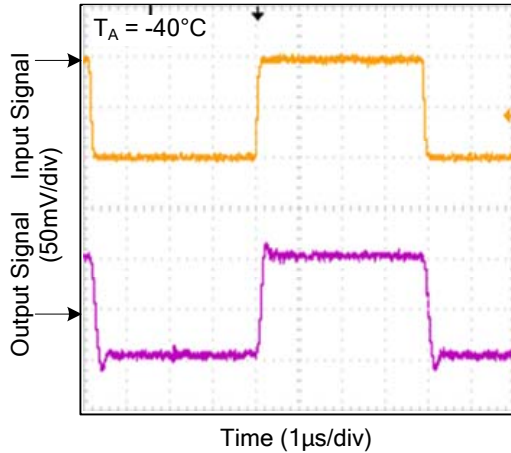
Non-Inverting Small Signal Pulse Response



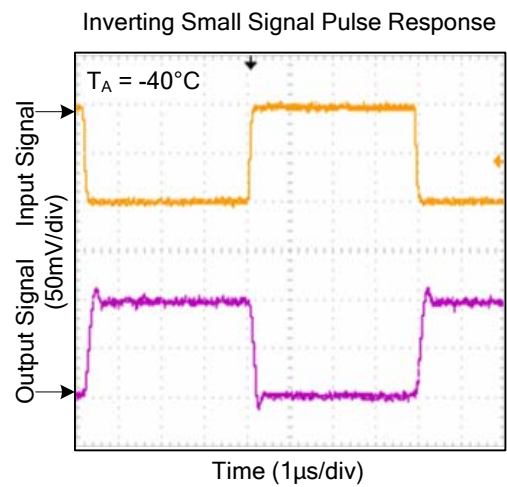
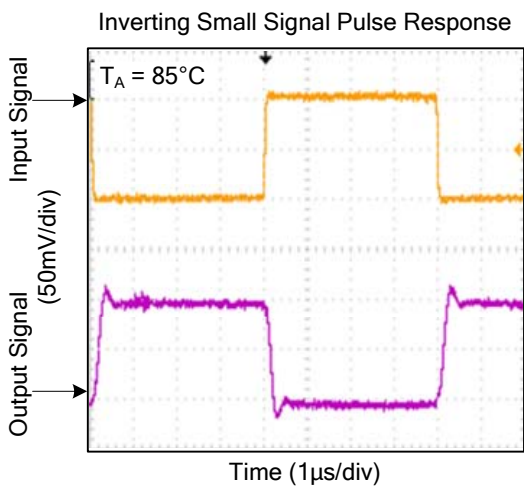
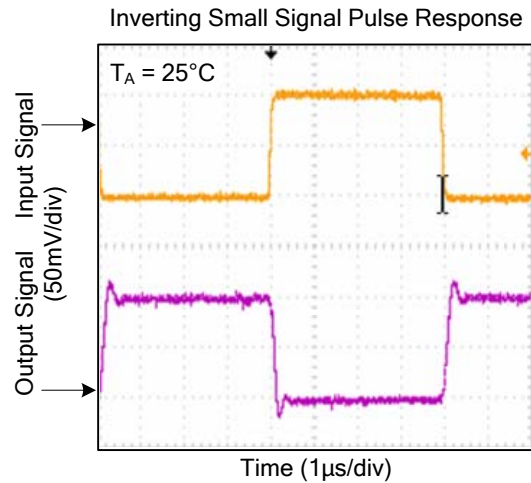
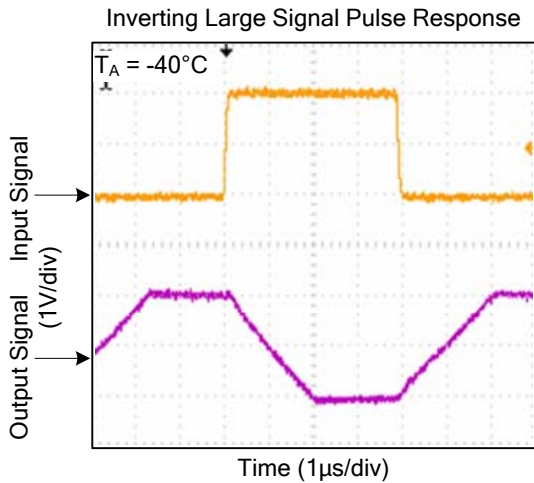
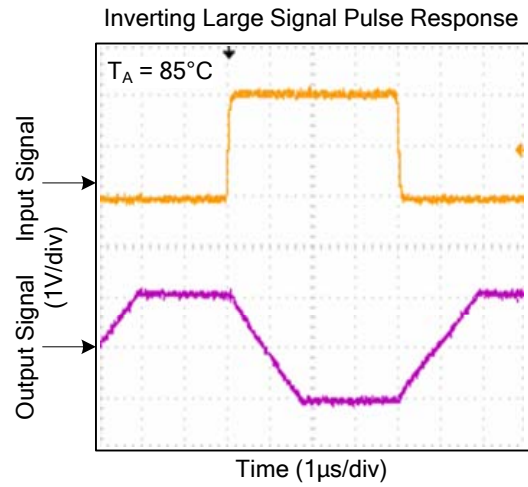
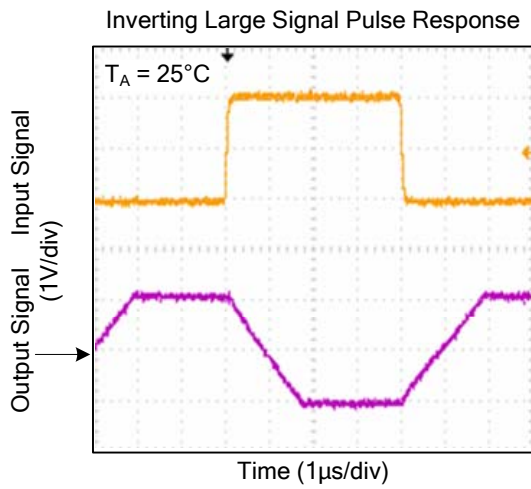
Non-Inverting Small Signal Pulse Response



Non-Inverting Small Signal Pulse Response



■ TYPICAL CHARACTERISTICS(Cont.)



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