



LM339

LINEAR INTEGRATED CIRCUIT

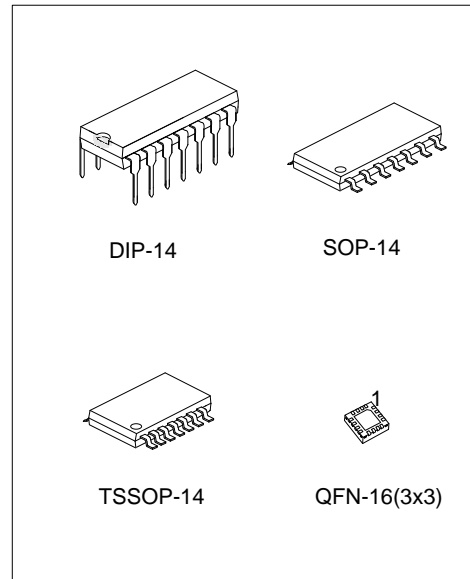
QUAD DIFFERENTIAL COMPARATOR

DESCRIPTION

The UTC LM339 consists of four independent voltage comparators, designed specifically to operate from a single power supply over a wide voltage range.

FEATURES

- *Signal or Dual Supply Operation.
- *Wide Operating Supply Range ($V_{CC}=2V\sim 36V$).
- *Input Common-Mode Voltage Includes Ground.
- *Low Supply Current Drain $I_F=0.8mA$ (Typical).
- *Open Collector Outputs for Wired and Connection.
- *Low Input Bias Current $I_{BIAS}=25nA$ (Typical).
- *Low Output Saturation Voltage.
- *Output Compatible with TTL, DTL, and CMOS Logic System.



ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen-Free		
LM339L-D14-T	LM339G-D14-T	DIP-14	Tube
LM339L-S14-R	LM339G-S14-R	SOP-14	Tape Reel
LM339L-P14-R	LM339G-P14-R	TSSOP-14	Tape Reel
LM339L-Q16-3030-R	LM339G-Q16-3030-R	QFN-16(3x3)	Tape Reel

<p>LM339G-D14-T</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) DIP: DIP-14, S14: SOP-14, P14: TSSOP-14 Q16-3030: QFN-16(3x3) (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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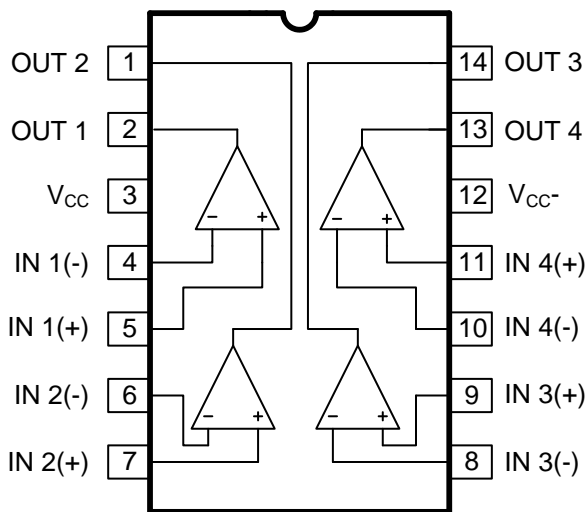
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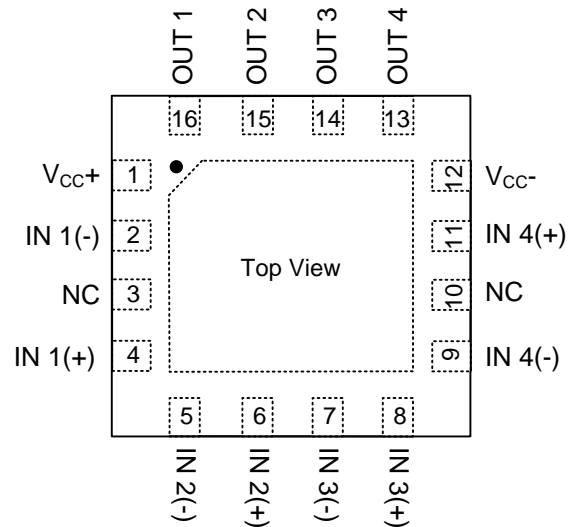
MARKING

PACKAGE	MARKING
DIP-14	<p> UTC □□□□ → Date Code L: Lead Free G: Halogen Free Lot Code </p>
SOP-14 TSSOP-14	<p> UTC □□□□ → Date Code L: Lead Free G: Halogen Free Lot Code </p>
QFN-16(3x3)	<p> UTC LM339 → L: Lead Free G: Halogen Free Lot Code ← Date Code </p>

PIN CONFIGURATION

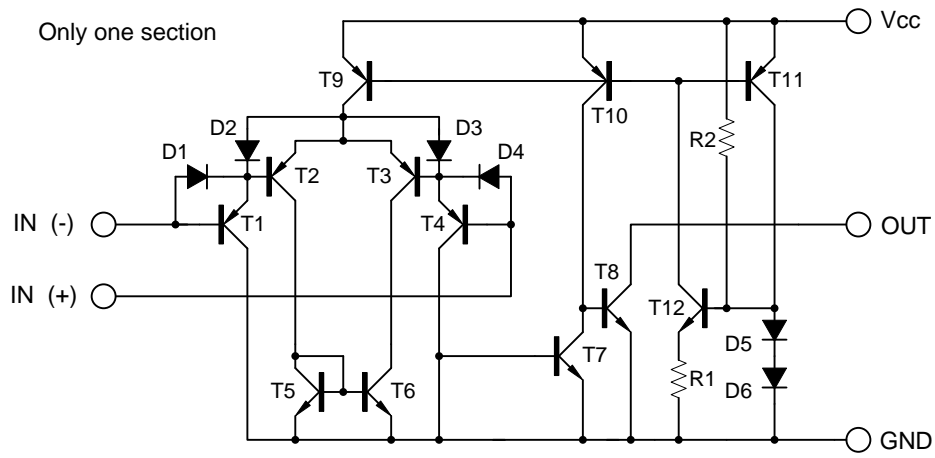


DIP-14/SOP-14/TSSOP-14



QFN-16(3x3)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V _{CC}	±18 or 36	V
Differential input Voltage		V _{I(DIFF)}	36	V
Input Voltage		V _{IN}	-0.3 ~ 36	V
Power Dissipation	DIP-14	P _D	760	mW
	SOP-14		560	mW
	TSSOP-14		440	mW
	QFN-16(3×3)		1300	mW
Junction Temperature		T _J	+150	°C
Operating Temperature		T _{OPR}	-40 ~ +125	°C
Storage Temperature		T _{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. It is guarantee by design, not 100% be tested.

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V, T_A=25°C, All voltage referenced to GND unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	V _{I(OFF)}	V _{CM} =0~V _{CC} -1.5, V _{OUT(P)} =1.4V, R _S =0		±1.5	±3.0	mV
Input Offset Current	I _{I(OFF)}			±2.3	±50	nA
Input Bias Current	I _{BIAS}			57	250	nA
Input Common-Mode Voltage Range	V _{IN(R)}		0		V _{CC} -1.5	V
Supply Current	I _{CC}	R _L =∞		1.1	2.0	mA
Large Signal Voltage Gain	G _V	V _{CC} =15V, R _L >15kΩ	50	200		V/mV
Large Signal Response Time	t _{RES}	V _{IN} =TTL logic wing V _{REF} =1.4V, V _{RL} =5V, R _L =5.1kΩ		350		ns
Response Time	t _{RES}	V _{RL} =5V, R _L =5.1kΩ		1400		ns
Output Sink Current	I _{SINK}	V _{IN(-)} >1V, V _{IN(+)} =0V, V _{OUT(P)} <1.5V	6	18		mA
Output Saturation Voltage	V _{SAT}	V _{IN(-)} >1V, V _{IN(+)} =0V, I _{SINK} =4mA		140	400	mV
Output Leakage Current	I _{LEAK}	V _{IN(+)} =1V, V _{IN(-)} =0V		0.1		nA
			V _{OUT(P)} =5V			1.0
Differential Input Voltage	V _{IN(DIFF)}				36	V

TYPICAL CHARACTERISTICS

Fig.1 Supply Current

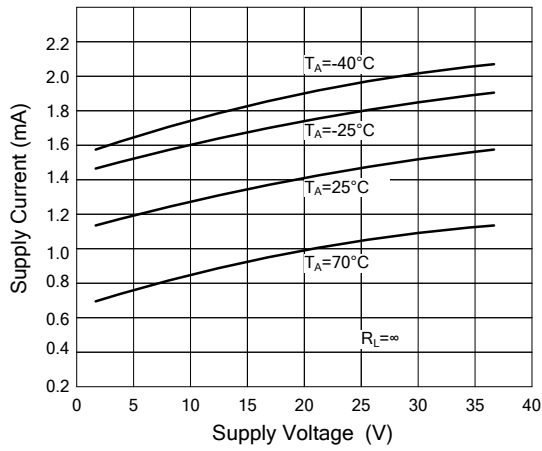


Fig.2 Input Current

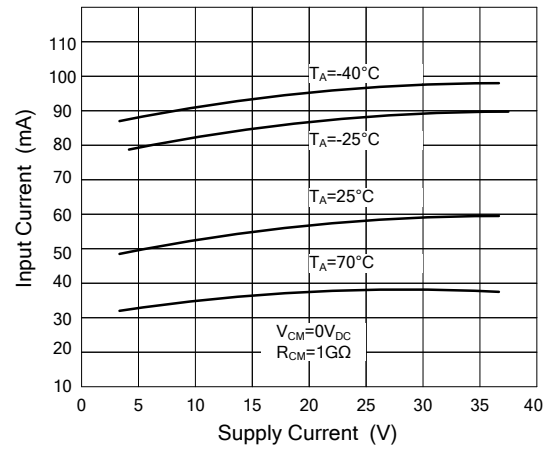


Fig.3 Output Saturation Voltage

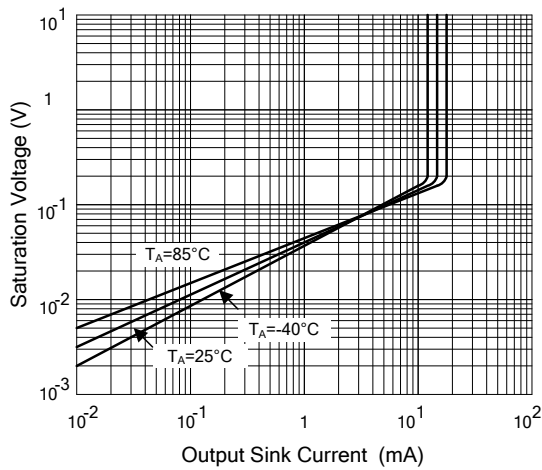


Fig.4 Reponse Time For Various Input Overdrive Negative Transition

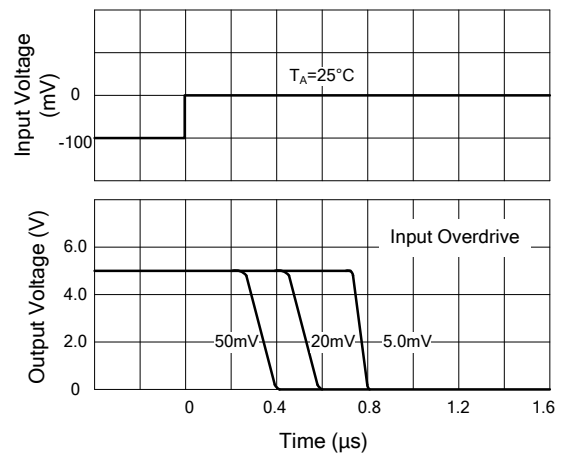
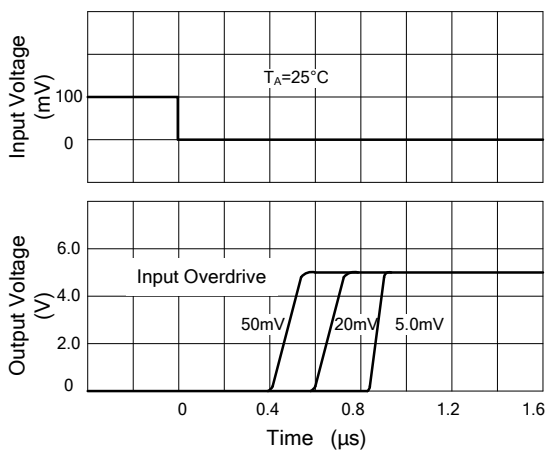


Fig.5 Reponse Time For Various Input Overdrive Positive Transition



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