



MJD210

PNP SILICON TRANSISTOR

PNP SILICON DPAK FOR SURFACE MOUNT APPLICATIONS

DESCRIPTION

The UTC MJD210 is designed for low voltage, low-power, high-gain audio amplifier applications.

FEATURE

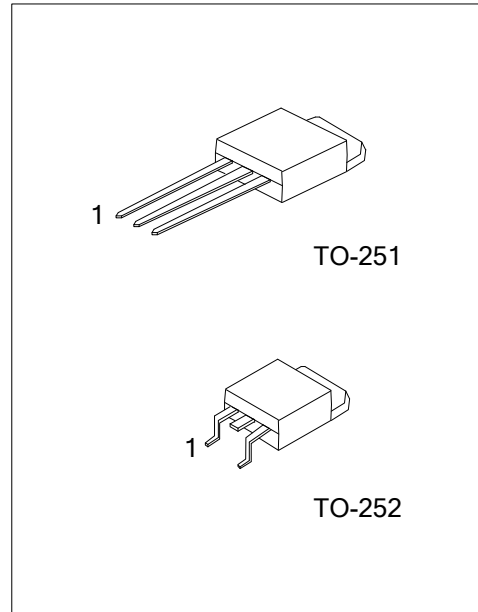
- * Collector-Emitter Sustaining Voltage
 $V_{CE(SUS)} = -25V$ (Min) @ $I_C = -10mA$
- * High DC Current Gain
 $h_{FE} = 70$ (Min) @ $I_C = -500mA$
 $= 45$ (Min) @ $I_C = -2A$
 $= 10$ (Min) @ $I_C = -5A$
- * Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- * Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- * Lead Formed Version in 16mm Tape and Reel ("T4" Suffix)
- * Low Collector – Emitter Saturation Voltage
 $V_{CE(SAT)} = -0.3V$ (Max) @ $I_C = -500mA$
 $= -0.75V$ (Max) @ $I_C = -2.0 A$
- * High Current-Gain-Bandwidth Product
 $f_T = 65$ MHz (Min) @ $I_C = -100 mA$
- * Annular Construction for Low Leakage
 $I_{CBO} = -100 nA$ @ Rated V_{CB}

NORDERING INFORMATIO

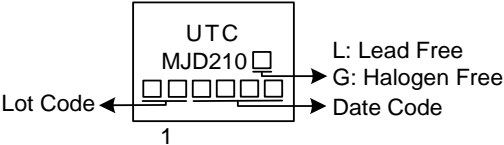
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
MJD210L-TM3-T	MJD210G-TM3-T	TO-251	B	C	E	Tube
MJD210L-TN3-R	MJD210G-TN3-R	TO-252	B	C	E	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

MJD210G-TM3-T	(1)Packing Type	(1) T: Tube, R: Tape Reel
	(2)Package Type	(2) TTM3: TO-251, TN3: TO-252
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free



■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Collector-Base Voltage		V _{CBO}	-40	V
Collector-Emitter Voltage		V _{CEO}	-25	V
Emitter-Base Voltage		V _{EBO}	-7	V
Collector Current	Continuous	I _C	-5	A
	Peak		-10	A
Base Current		I _B	-1	A
Total Device Dissipation	T _C =25°C	P _D	12.5	W
	Derate above 25°C		0.1	W/°C
	T _A =25°C (Note2)		1.4	W
	Derate above 25°C		0.011	W/°C
Junction Temperature		T _J	+150	°C
Storage Junction Temperature		T _{STG}	-65 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. When surface mounted on minimum pad sizes recommended.

■ THERMAL DATA (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ _{JA}	89.3	°C/W
Junction to Case	θ _{JC}	10	°C/W

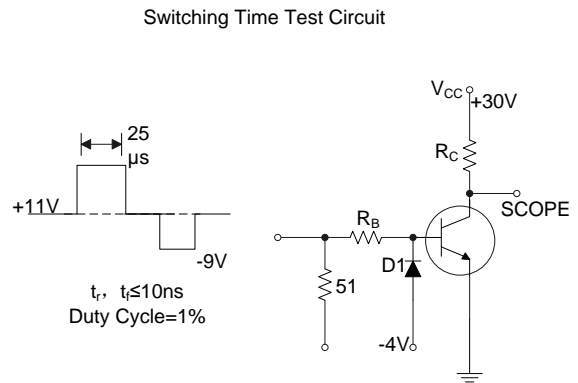
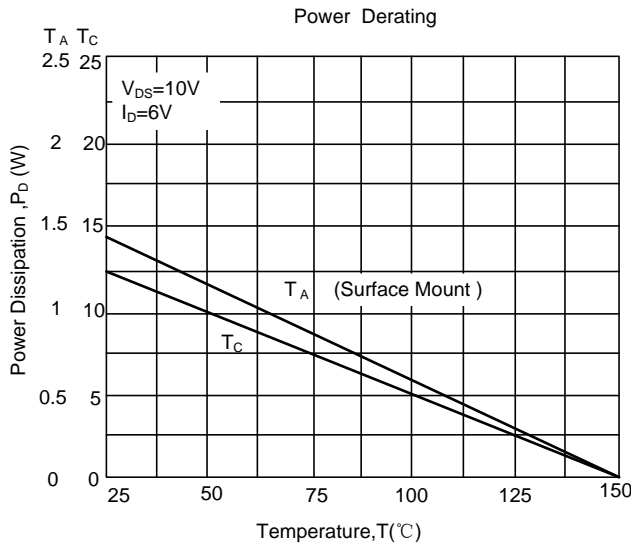
■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage(Note 1)	V _{CEO(SUS)}	I _C =-10mA, I _B =0	-25			V
Collector Cutoff Current	I _{CBO}	V _{CB} =-40V, I _E =0			-100	nA
		V _{CB} =-40V, I _E =0, T _J =125°C			-100	nA
Emitter Cutoff Current	I _{EBO}	V _{BE} =-7V, I _C =0			-100	nA
ON CHARACTERISTICS						
DC Current Gain (Note 1)	h _{FE}	I _C =-500mA, V _{CE} =-1V	70			
		I _C =-2A, V _{CE} =-1V	45		180	
		I _C =-5A, V _{CE} =-2V	10			
Collector-Emitter Saturation Voltage (Note 1)	V _{CE(SAT)}	I _C =-500mA, I _B =-50mA			-0.3	V
		I _C =-2A, I _B =-200mA			-0.75	
		I _C =-5A, I _B =-1A			-1.8	
Base-Emitter Saturation Voltage (Note 1)	V _{BE(SAT)}	I _C =-5A, I _B =-1A			-2.5	V
Base-Emitter On Voltage (Note 1)	V _{BE(ON)}	I _C =-2A, V _{CE} =-1V			-1.6	V
DYNAMIC CHARACTERISTICS						
Current-Gain-Bandwidth Product (Note 2)	f _T	I _C =-100mA, V _{CE} =-10V, f _{TEST} = 10MHz	65			MHz
Output Capacitance	C _{OB}	V _{CB} =-10V, I _E =0, f=0.1MHz			120	pF

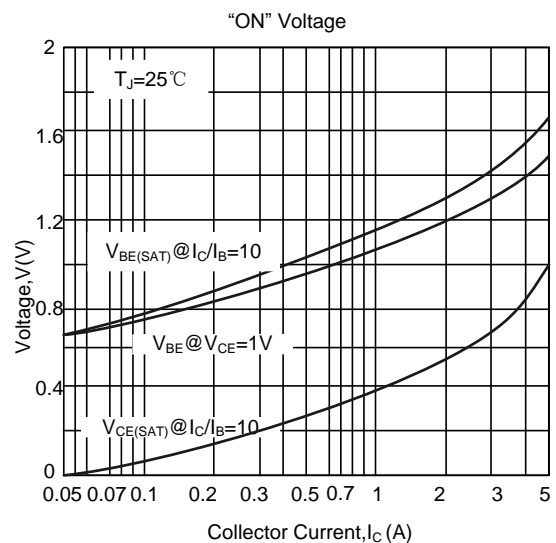
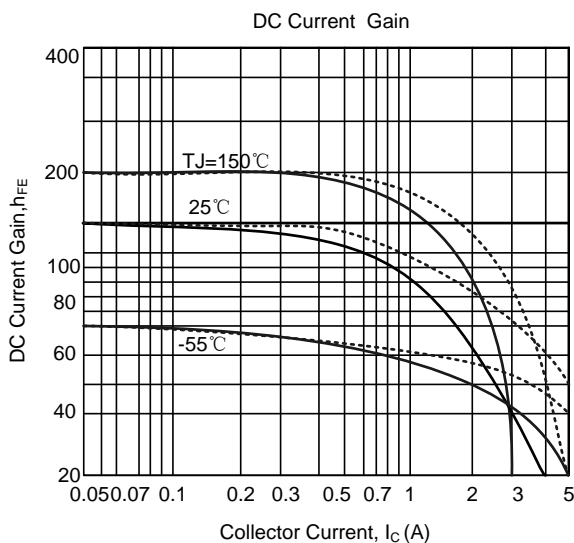
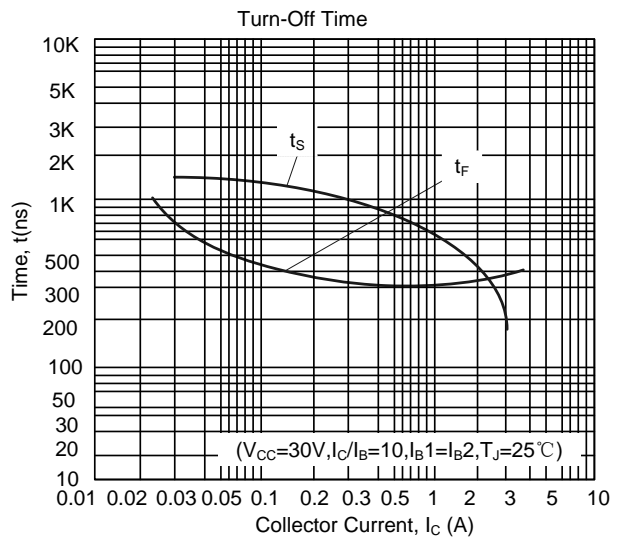
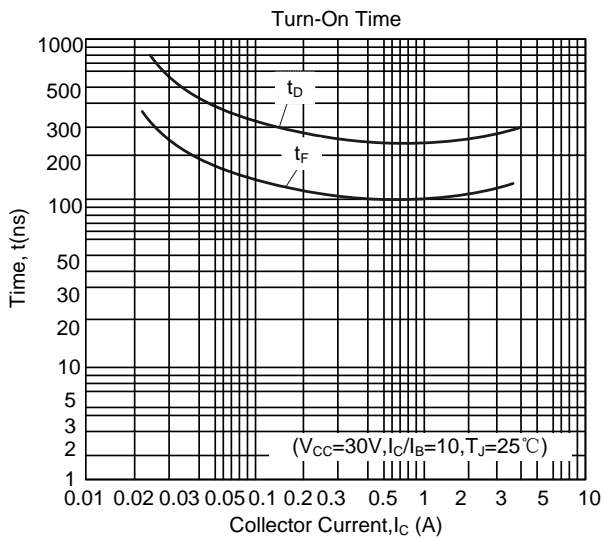
Note: 1. Pulse Test: Pulse Width = 300μs, Duty Cycle ≈ 2%.

2. $f_T = |h_{FE}| \cdot f_{TEST}$.

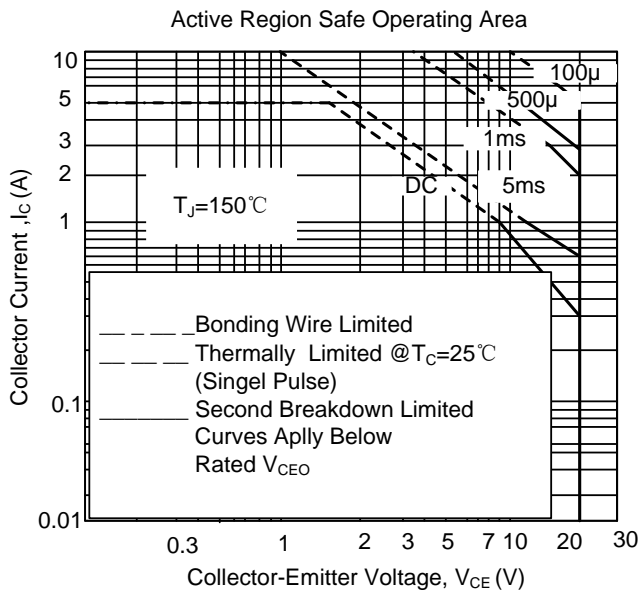
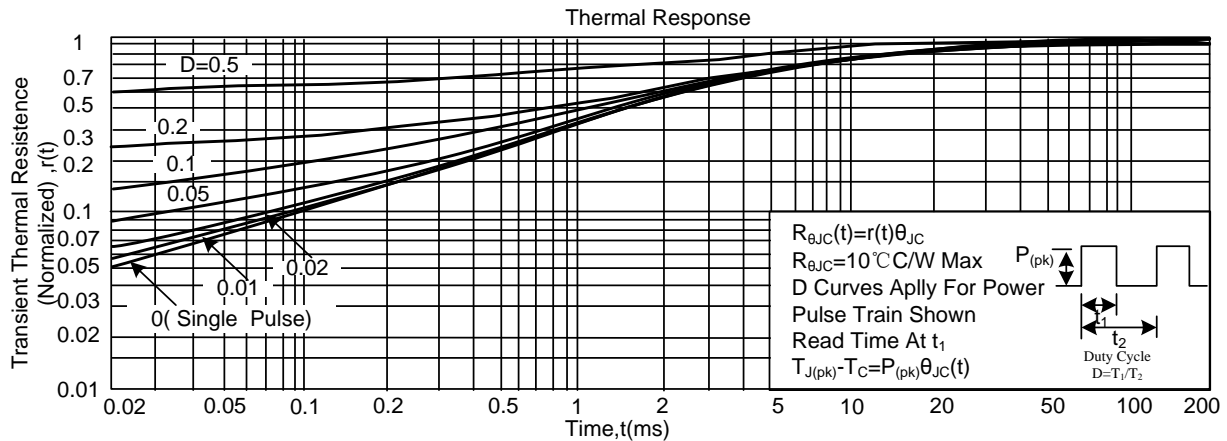
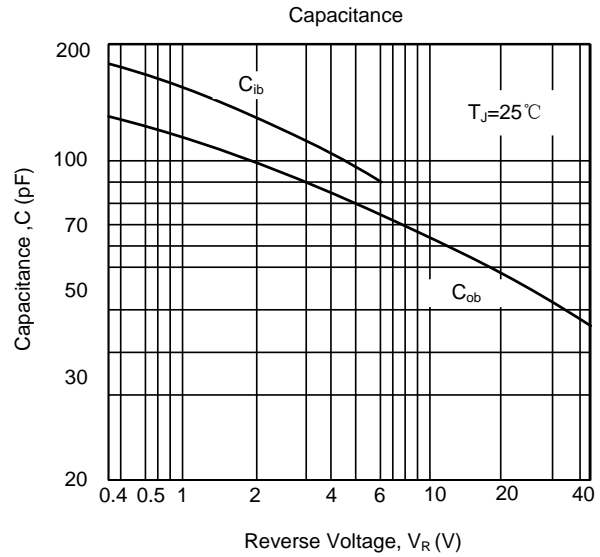
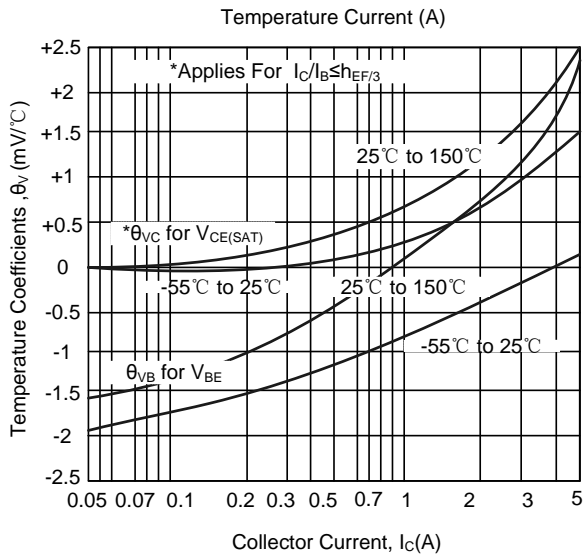
TYPICAL CHARACTERISTICS



R_B and R_C Varied to Obtain Desired Current Levels
 $D1$ Must be Fast Recovery Type, e.g.:
 1N5825 Used Above $I_B \approx 100mA$ for PNP Test
 Circuit MSD6100 Used Below $I_B \approx 100mA$ Reverse
 All Polarities



TYPICAL CHARACTERISTICS (Cont.)



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_c - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Fig. 9 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_c is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} = 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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