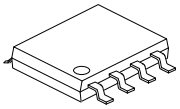
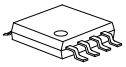
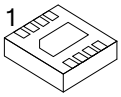
1.7-W MONO FULLY DIFFERENTIAL AUDIO POWER AMPLIFIER



SOP-8



MSOP-8



DFN3030-8

■ DESCRIPTION

The UTC **PA6204** is a mono fully-differential audio amplifier, capable of delivering 1.7W of continuous average power to an 8-Ω BTL load with less than 10% distortion from a 5V power supply.

The UTC **PA6204** is ideal for PDA/smart phone applications due to features such as -80-dB supply voltage rejection from 20Hz to 2kHz, improved RF rectification immunity, small 20mm^2 total PCB area, and a fast startup with minimal pop. The device operates from 2.5V to 5.5V, drawing only 4mA of quiescent supply current.

The UTC **PA6204** is suitable for diverse applications, such as PDAs, Wireless or cellular handsets, Portable devices.

■ FEATURES

* 1.7W into 8Ω from a 5-V supply at THD=10% (Typ.)
* 2.5V-5.5V operation
* Low supply current: 4mA typ at 5V
* Ultra low current shutdown mode
* Only three external components
  - Improved PSRR (-80dB) for direct battery operation
  - Fully differential design reduces RF rectification
  - -63dB CMRR eliminates two input coupling capacitors
* Fast startup with minimal pop

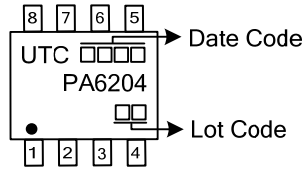
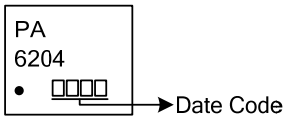
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
PA6204L-S08-R	PA6204G-S08-R	SOP-8	Tape Reel
PA6204L-SM1-R	PA6204G-SM1-R	MSOP-8	Tape Reel
PA6204L-K08-3030-R	PA6204G-K08-3030-R	DFN3030-8	Tape Reel

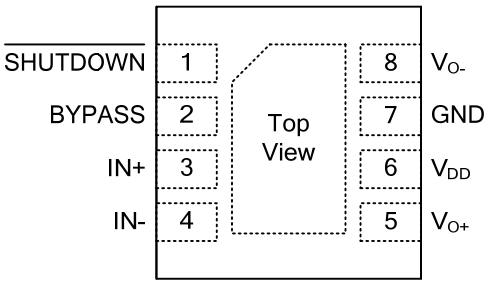
PA6204G-S08-R
(1) Packing Type
(2) Package Type
(3) Green Package

(1) R: Tape Reel, T: Tube
(2) S08: SOP-8, SM1: MSOP-8, K08-3030:DFN3030-8
(3) G: Halogen Free and Lead Free, L: Lead Free

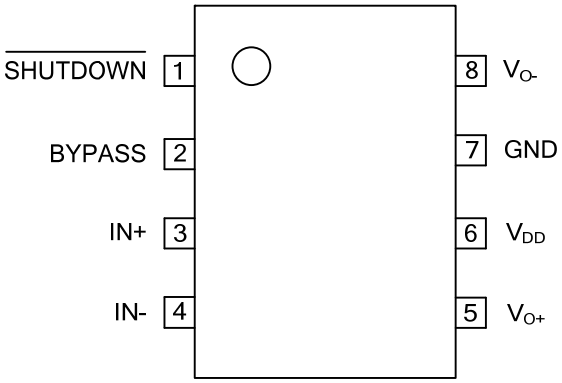
■ MARKING

SOP-8 / MSOP-8	DFN3030-8
	

■ PIN CONFIGURATION



DFN3030-8

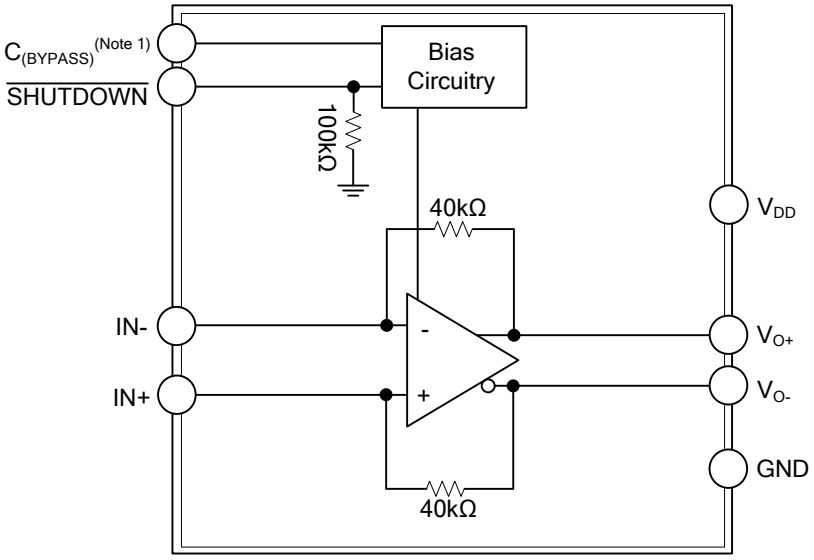


SOP-8 / MSOP-8

■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	$\overline{\text{SHUTDOWN}}$	Shutdown Terminal (Active Low Logic)
2	BYPASS	Mid-supply Voltage, Adding a Bypass Capacitor Improves PSRR
3	IN+	Positive Differential Input
4	IN-	Negative Differential Input
5	V_{O+}	Positive BTL Output
6	V_{DD}	Power Supply
7	GND	High-current Ground
8	V_{O-}	Negative BTL Output

■ BLOCK DIAGRAM



Note 1. $C_{(BYPASS)}$ is optional.

■ ABSOLUTE MAXIMUM RATING (Over operating free-air temperature range unless otherwise noted)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 ~ 6	V
Input Voltage	V_I	-0.3 ~ V_{DD}+0.3	V
Power Dissipation (T_A=25°C)	P_D	Internally Limited	W
Junction Temperature	T_J	-40 ~ +150	°C
Operating Free-air Temperature	T_A	-40 ~ +85	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Derating factor based on high-k board layout.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	θ_{JA}	140	°C/W
	MSOP-8		210	°C/W
	DFN3030-8		59	°C/W
Junction to Case	SOP-8	θ_{JC}	35	°C/W
	MSOP-8		56	°C/W
	DFN3030-8		4.3 (Note)	°C/W

Note: Surface mounted on 1 in ^{2} copper pad of FR4 board.

■ RECOMMENDED OPERATING CONDITIONS

PACKAGE		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{DD}	2.5		5.5	V
High-level Input Voltage	$\overline{SHUTDOWN}$	V_{IH}	1.55			V
Low-level Input Voltage	$\overline{SHUTDOWN}$	V_{IL}			0.5	V
Operating Free-air Temperature		T_A	-40		85	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output Offset Voltage (Measured Differentially)	V_{OS}	V_I=0V differential, Gain=1V/V, V_{DD}=5.5V		-9	0.3	9	mV
Power Supply Rejection Radio	PSRR	V_{DD}=2.5V~5.5V			-85	-60	dB
Common Mode Input Range	V_{IC}	V_{DD}=2.5V~5.5V		0.5		V_{DD}-0.8	V
Common Mode Rejection Ratio	CMRR	V_{DD}=5.5V, V_{IC}=0.5V~4.7V			-63	-40	dB
		V_{DD}=2.5V, V_{IC}=0.5V~1.7V			-63	-40	
Low-Output Swing		R_L=8Ω, Gain=1V/V V_{IN+}=0V, V_{IN-}=V_{DD}	V_{DD}=5.5V		0.45		V
			V_{DD}=3.6V		0.37		
			V_{DD}=2.5V		0.26	0.4	
High-Output Swing		R_L=8Ω, Gain=1V/V V_{IN+}=V_{DD}, V_{IN-}=0V	V_{DD}=5.5V		4.95		V
			V_{DD}=3.6V		3.18		
			V_{DD}=2.5V	2	2.13		
High-Level Input Current, $\overline{SHUTDOWN}$	$\|I_{IH}\|$	V_{DD}=5.5V, V_I=5.8V			58	100	μA
Low-Level Input Current, $\overline{SHUTDOWN}$	$\|I_{IL}\|$	V_{DD}=5.5V, V_I=-0.3V			3	100	μA
Quiescent Current	I_Q	V_{DD}=2.5V~5.5V, No Load			4	6	mA
Supply Current	$I_{(SD)}$	$V_{(\overline{SHUTDOWN})}$≤0.5V, V_{DD}=2.5V~5.5V, R_L=8Ω			0.01	1	μA
Gain		R_L=8Ω		$\frac{38k\Omega}{R_I}$	$\frac{40k\Omega}{R_I}$	$\frac{42k\Omega}{R_I}$	V/V
Resistance From Shutdown To GND					100		kΩ

■ OPERATING CHARACTERISTICS (T_A=25°C, Gain=1V/V, unless otherwise specified)

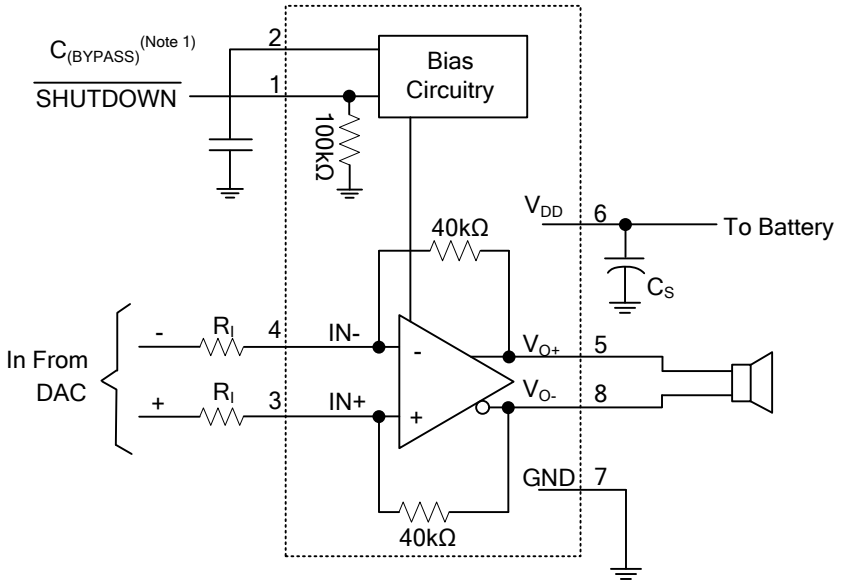
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output Power	P_O	THD+N=1%, f=1kHz, R_L=8Ω	V_{DD}=5V		1.36		W
			V_{DD}=3.6V		0.72		
			V_{DD}=2.5V		0.33		
		THD+N=10%, f=1kHz, R_L=8Ω	V_{DD}=5V		1.7		W
			V_{DD}=3.6V		0.85		
			V_{DD}=2.5V		0.4		
Total Harmonic Distortion Plus Noise	THD+N	V_{DD}=5V, P_O=1W, R_L=8Ω, f=1kHz			0.02		%
		V_{DD}=3.6V, P_O=0.5W, R_L=8Ω, f=1kHz			0.02		
		V_{DD}=2.5V, P_O=200mW, R_L=8Ω, f=1kHz			0.03		
Supply Ripple Rejection Ratio	K_{SVR}	V_{DD}=3.6V, Inputs Ac-grounded With C_I=2μF, $V_{(RIPPLE)}$=200mV_{pp}	f=217Hz		-80		dB
			f=20Hz~20kHz		-70		
Signal-To-Noise Radio	SNR	V_{DD}=5V, P_O=1W, R_L=8Ω			105		dB
Output Voltage Noise	V_N	V_{DD}=3.6V, f=20Hz~20kHz, Inputs Ac-grounded With C_I=2μF	No Weighting		15		μV_{RMS}
			A Weighting		12		
Common Mode Rejection Radio	CMRR	V_{DD}=3.6V, V_{IC}=1V_{PP}	f=217Hz		-65		dB
Feedback Resistance	R_F			38	40	44	kΩ
Start-up Time From Shutdown		V_{DD}=3.6V, C_{BYPASS}=0.1μF			27		ms

■ TYPICAL APPLICATION CIRCUIT

Table 1. Typical Component Values

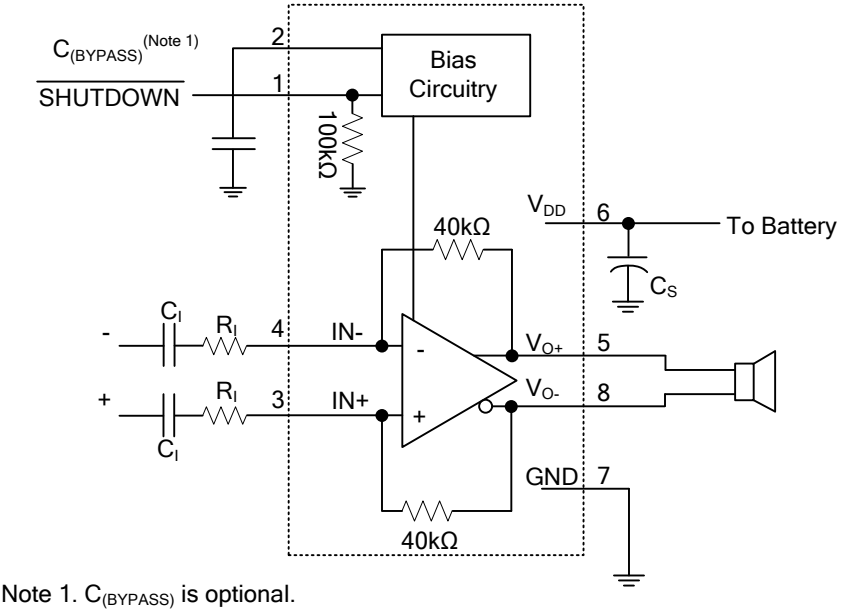
COMPONENT	VALUE	UNIT
RI	40	kΩ
$C_{(BYPASS)}$ (Note 1)	0.22	μF
C_S	1	μF
C_I	0.22	μF

Note: 1. $C_{(BYPASS)}$ is optional



Note 1. $C_{(BYPASS)}$ is optional.

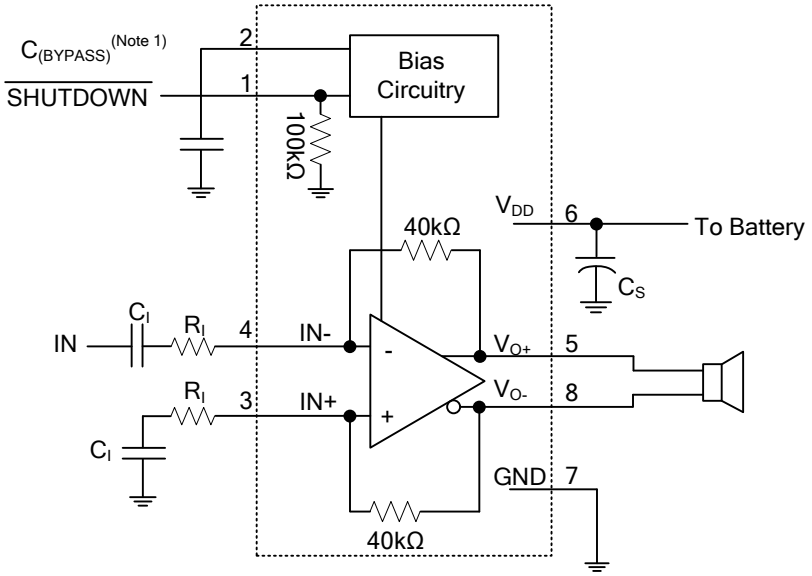
Figure 1. Typical Differential Input Application Schematic



Note 1. $C_{(BYPASS)}$ is optional.

Figure 2. Differential Input Application Schematic Optimized With Input Capacitors

■ TYPICAL APPLICATION CIRCUIT(Cont.)



Note 1. $C_{(BYPASS)}$ is optional.

Figure 3. Single-Ended Input Application Schematic