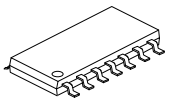
U74AC74

CMOS IC

DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET



SOP-14

■ DESCRIPTION

The **U74AC74** is a dual positive-edge-triggered D-type flip-flop.

The preset ($\overline{PRE}$) and clear ($\overline{CLR}$) input can set or reset the output at a low level ,regardless of the level of others inputs .when the $\overline{PRE}$ and $\overline{CLR}$ are inactive(high), data at the data D input meeting the set-up time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Following the hold-time interval, data D can be changed without affecting the levels at the outputs.

■ FEATURES

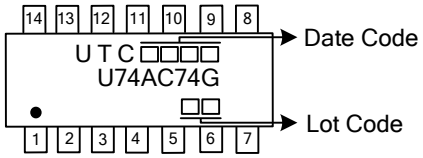
* Operating voltage rauge: V_{CC}(OPR)=2V to 6V.
* Inputs accept voltages to 6V
* Max tpd at 10ns of 5V

■ ORDERING INFORMATION

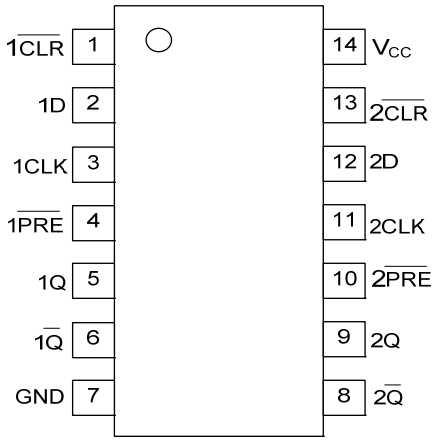
Ordering Number	Package	Packing
U74AC74G-S14-R	SOP-14	Tape Reel

U74AC74G-S14-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S14: SOP-14 (3) L: Lead Free, G: Halogen Free and Lead Free

■ MARKING



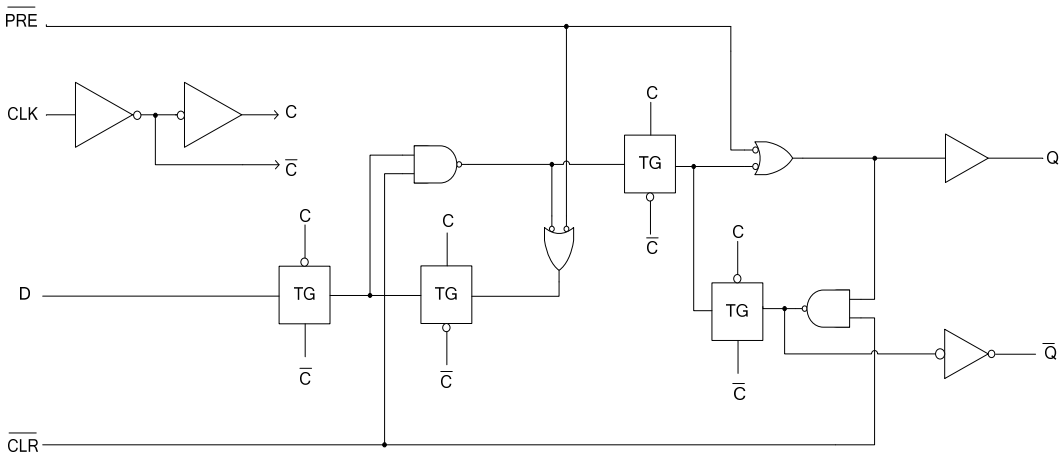
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT				OUTPUT	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	Q0

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7	V
Input Voltage	V_{IN}	-0.5~ V_{CC}+0.5	V
Output Voltage(active mode)	V_{OUT}	-0.5~V_{CC}+0.5	V
Input Clamp Current(V_{IN}<0)	I_{IK}	-20(MIN)	mA
Output Clamp Current(V_{OUT}<0)	I_{OK}	±20	mA
Output Current	I_{OUT}	±50	mA
V_{CC} or GND Current	I_{CC}	±200	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2		6	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
High-level input voltage	V_{IH}	V_{CC} =3V	2.1			V
		V_{CC}=4.5V	3.15			
		V_{CC} =5.5V	3.85			
Low-level input voltage	V_{IL}	V_{CC}=3V			0.9	V
		V_{CC} =4.5V			1.35	
		V_{CC}=5.5V			1.65	
High-level Output Current	I_{OH}	V_{CC} =3V			-12	mA
		V_{CC}=4.5V			-24	
		V_{CC} =5.5V			-24	
Low-level Output Current	I_{OL}	V_{CC}=3V			12	mA
		V_{CC} =4.5V			24	
		V_{CC}=5.5V			24	
Input Transition Rise or Fall Rate	Δt/Δv				8	ns/V
Operating Temperature	T_A		-40		+85	°C

■ STATIC CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	I_{OH}=-50uA	V_{CC}=3V	2.9			V
			V_{CC}=4.5V	4.4			
			V_{CC}=5.5V	5.4			
		I_{OH}=-12mA	V_{CC}=3V	2.56			
		I_{OH}=-24mA	V_{CC}=4.5V	3.86			
			V_{CC}=5.5V	4.86			
Low-Level Output Voltage	V_{OL}	I_{OL}=-50uA	V_{CC}=3V			0.1	V
			V_{CC}=4.5V			0.1	
			V_{CC}=5.5V			0.1	
		I_{OL}=12mA	V_{CC}=3V			0.36	
		I_{OL}=24mA	V_{CC}=4.5V			0.36	
			V_{CC}=5.5V			0.36	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC} =0V ~ 5.5V, V_{IN}=V_{CC} or GND				±0.1	μA
Quiescent Supply Current	I_{CC}	V_{CC} = 5.5V, V_{IN}=5.5V or GND I_{OUT}=0				2	
Input Capacitance	C_{IN}	V_{CC} =3.3V, V_{IN}=V_{CC} or GND			3		pF

■ DYNAMIC CHARACTERISTICS

T_A=25°C, unless otherwise specified, Input: t_R, t_F≤2.5ns; PRR≤1MHz

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock frequency	F_{CLOCK}	V_{CC}=3V±0.3V			100	MH_Z
Pulse duration	tw	V_{CC}=3V±0.3V, $\overline{PRE}$ or $\overline{CLR}$ in Low	5.5			ns
		V_{CC}=3V±0.3V, CLK	5.5			
Setup time before CLK↑	tsu	V_{CC}=3V±0.3V, $\overline{PRE}$ or $\overline{CLR}$ inactive	0			ns
		Data	4			
Hold time ,data after CLK↑	th	V_{CC}=3V±0.3V	0.5			ns
Clock frequency	F_{CLOCK}	V_{CC}=5V±0.5V			140	MHz
Pulse duration	tw	V_{CC}=5V±0.5V, $\overline{PRE}$ or $\overline{CLR}$ in Low	4.5			ns
		V_{CC}=3V±0.3V, CLK	4.5			
Setup time before CLK↑	tsu	V_{CC}=5V±0.5V, $\overline{PRE}$ or $\overline{CLR}$ inactive	0			ns
		Data	3			
Hold time ,data after CLK↑	th	V_{CC}=5V±0.5V	0.5			ns

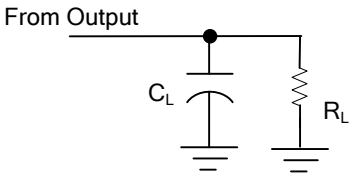
■ DYNAMIC CHARACTERISTICS (See Fig. 1 and Fig. 2 for test circuit and waveforms.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum clock	F_{MAX}	V_{CC}=3V±0.3V, C_L=50pF, R_L=500Ω	100	125		MHz
Propagation delay from input ($\overline{PRE}$ or $\overline{CLR}$) to output(Q or Q)	t_{PLH}	V_{CC}=3V±0.3V, C_L=50pF, R_L=500Ω	3.5	8	12	ns
	t_{PHL}		4	10.5	12	
Propagation delay from input (CLK) to output(Q or Q)	t_{PLH}	V_{CC}=3V±0.3V, C_L=50pF, R_L=500Ω	4.5	8	13.5	ns
	t_{PHL}		3.5	8	14	
Maximum clock	F_{MAX}	V_{CC}=5V±0.5V	140	160		MHz
Propagation delay from input ($\overline{PRE}$ or $\overline{CLR}$) to output(Q or $\overline{Q}$)	t_{PLH}	V_{CC}=5V±0.5V, C_L=50pF, R_L=500Ω	2.5	6	9	ns
	t_{PHL}		3	8	9.5	
Propagation delay from input (CLK) to output(Q or $\overline{Q}$)	t_{PLH}	V_{CC}=5V±0.5V, C_L=50pF, R_L=500Ω	3.5	6	10	ns
	t_{PHL}		2.5	6	10	

OPERATING CHARACTERISTICS

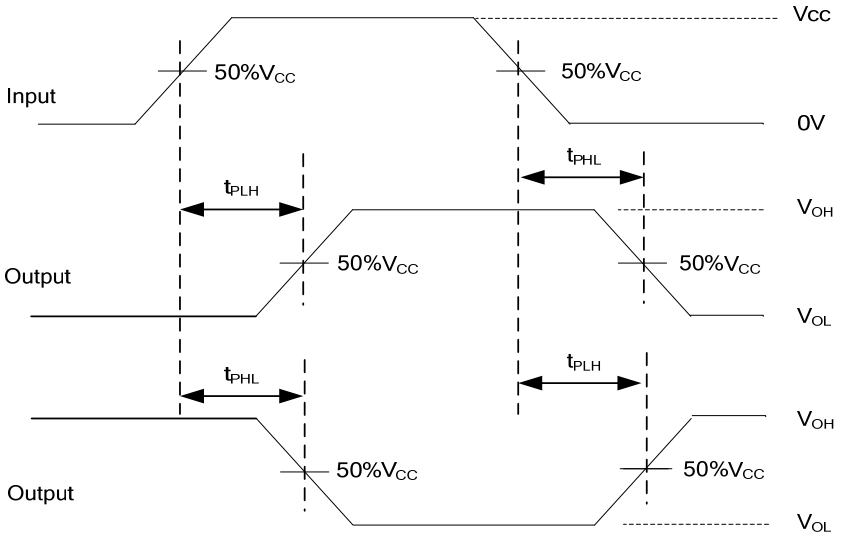
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Cpd	C_L=50p, f=1MHz, V_{CC}=3.3V		45		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

Note: C_L includes probe and jig capacitance.



PROPAGATION DELAY TIMES

Fig. 1 Load circuitry for switching times.

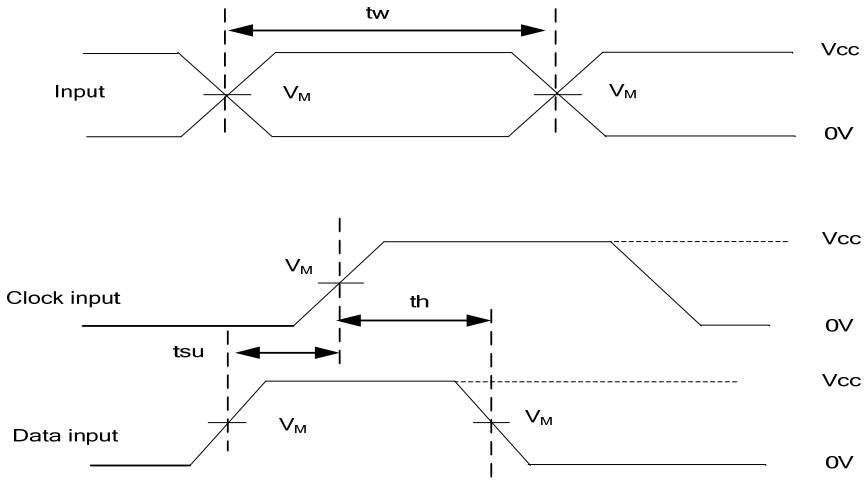


Fig. 2 Propagation delay from input to output and input voltage waveforms.