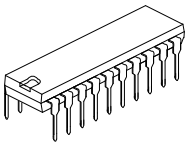
U74AHCT373

CMOS IC

OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS



DIP-20

TSSOP-20

■ DESCRIPTION

The **U74AHCT373** is an octal transparent D-type latch with 3-state outputs and 8 channels.

When the $\overline{OE}$ input is low and the LE input is high, the Q outputs follow the D inputs. When $\overline{OE}$ is low and LE is low, the Q outputs are latched at the logic levels of the D inputs.

When the $\overline{OE}$ input is high, the outputs are in the high-impedance. The $\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

■ FEATURES

* Inputs are TTL-Voltage Compatible
* Operate from 4.5V to 5.5V
* Inputs Accept Voltages to 5.5V
* Max t_{PD} of 8.5ns at V_{CC}=5V, C_L=15pF

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHCT373L-D20-T	U74AHCT373G-D20-T	DIP-20	Tube
-	U74AHCT373G-P20-R	TSSOP-20	Tape Reel

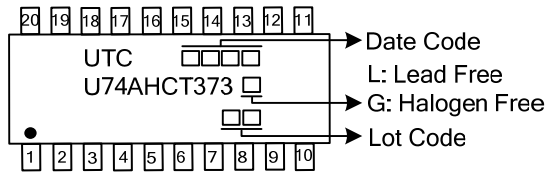
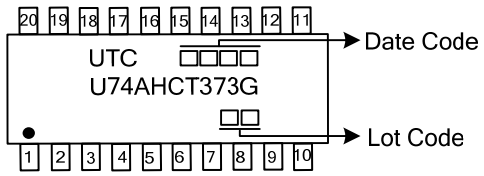
U74AHCT373L-D20-T

(1)Packing Type — (1) T: Tube, R: Tape Reel

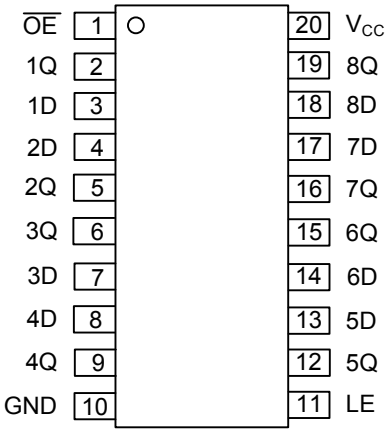
(2)Package Type — (2) D20: DIP-20, P20: TSSOP-20

(3)Green Package — (3) L: Lead Free, G: Halogen Free and Lead Free

■ MARKING

DIP-20	TSSOP-20
	

■ PIN CONFIGURATION

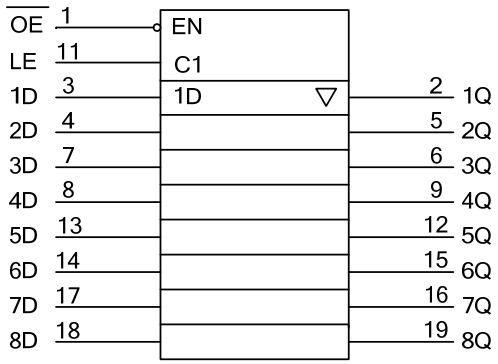


■ FUNCTION TABLE

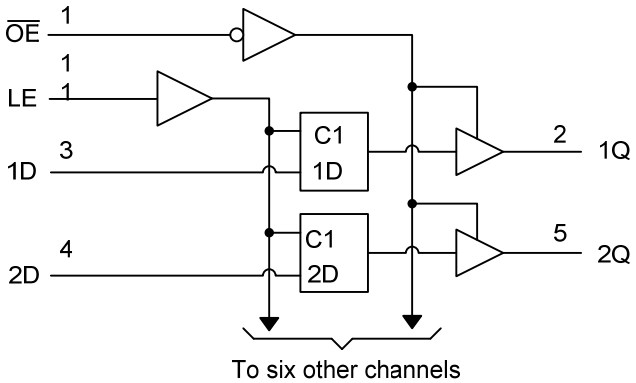
INPUTS($\overline{OE}$)	INPUTS(LE)	INPUTS(D)	OUTPUT(Q)
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Note: H: HIGH voltage level; L: LOW voltage level.

■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
Input Voltage Range (Note 3)	V_I	-0.5 ~ 7	V
Output Voltage Range (Note 3)	V_O	-0.5 ~ V_{CC} +0.5	V
Input Clamp Current	I_{IK}	-20	mA
Output Clamp Current	I_{OK}	±20	mA
Output Current	I_O	±25	mA
V_{CC} or GND Current	I_{CC}	±75	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.
2. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	4.5		5.5	V
High-Level Input Voltage	V_{IH}	2			V
Low-Level Input Voltage	V_{IL}			0.8	V
Input Voltage	V_{IN}	0		5.5	V
Output Voltage	V_{OUT}	0		V_{CC}	V
High-Level Output Current	I_{OH}			-8	mA
Low-Level Output Current	I_{OL}			8	mA
Input Rise or Fall Times	t_R, t_F			20	ns/V
Operating free-air temperature	T_A	-40		85	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	V_{OH}	V_{CC}=4.5V, I_{OH}=-50μA	4.4	4.5		V
		V_{CC}=4.5V, I_{OH}=-8mA	3.94			
Output Voltage Low-Level	V_{OL}	V_{CC}=4.5V, I_{OL}=50μA			0.1	V
		V_{CC}=4.5V, I_{OL}=8mA			0.36	
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=0V to 5.5V, V_{IN}=0 or 5.5V			±0.1	μA
Leakage Current (For output in high-impedance state)	I_{OZ}	V_{CC}=5.5V, V_{IN}=V_{IH} or V_{IH}, V_{OUT}=0 or 5.5V			±0.25	μA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0			4	μA
Additional Quiescent Supply Current	ΔI_{CC}	V_{CC}=5.5V, one input at 3.4V, Other inputs at V_{CC} or GND			1.35	mA
Input Capacitance	C_I	V_{CC}=5V, V_{IN}=V_{CC} or GND		4	10	pF
Output Capacitance	C_O	V_{CC}=5V, V_{OUT}=V_{CC} or GND		9		pF

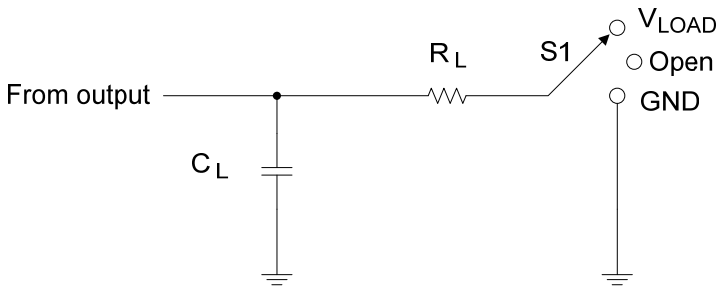
■ SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From D to Q	t_{PLH}/t_{PHL}	V_{CC}=5V±0.5V, C_L=15pF		5.1	8.5	ns
		V_{CC}=5V±0.5V, C_L=50pF		5.9	9.5	
From LE to Q		V_{CC}=5V±0.5V, C_L=15pF		7.7	12.3	
		V_{CC}=5V±0.5V, C_L=50pF		8.5	13.3	
From $\overline{OE}$ to Q	t_{PZL}/t_{PZH}	V_{CC}=5V±0.5V, C_L=15pF		6.3	10.9	ns
		V_{CC}=5V±0.5V, C_L=50pF		7.1	11.9	
From $\overline{OE}$ to Q	t_{PLZ}/t_{PHZ}	V_{CC}=5V±0.5V, C_L=15pF		6	10.2	ns
		V_{CC}=5V±0.5V, C_L=50pF		6.8	11.2	
Pulse Width, LE High	t_W	V_{CC}=5V±0.5V	6.5			ns
Setup Time, Data Before LE↓	t_{SU}	V_{CC}=5V±0.5V	1.5			ns
Hold Time, Data After LE↓	t_H	V_{CC}=5V±0.5V	3.5			ns

■ OPERATING CHARACTERISTICS (T_A=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load, f=1MHz		17		pF

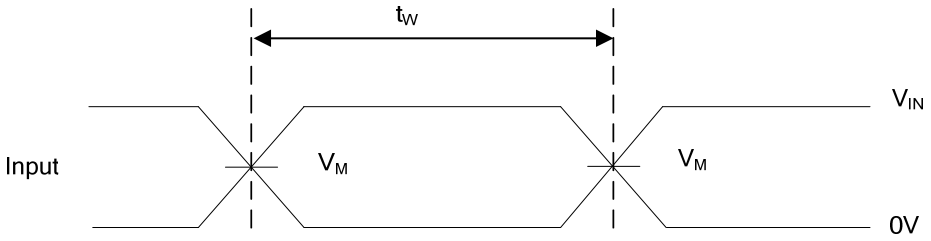
■ TEST CIRCUIT AND WAVEFORMS



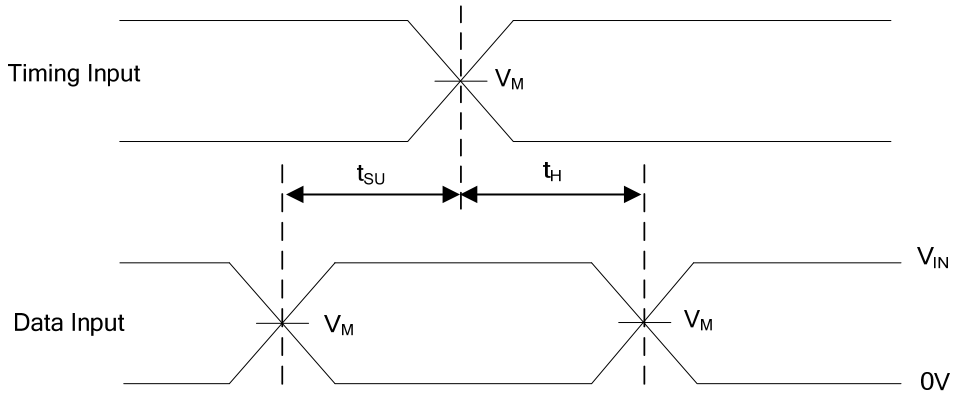
Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	Input		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_{IN}	t_R, t_F					
5V±0.5V	V_{CC}	≤3ns	$V_{CC}/2$	V_{CC}	15pF 50pF	1kΩ	0.5V

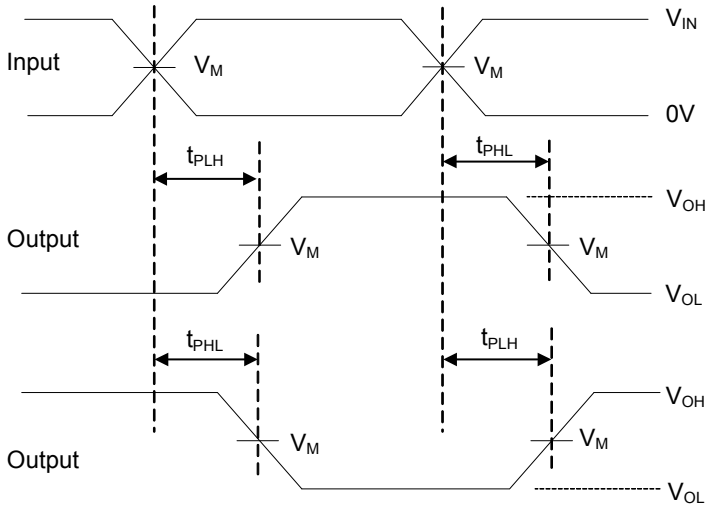


Pulse Duration

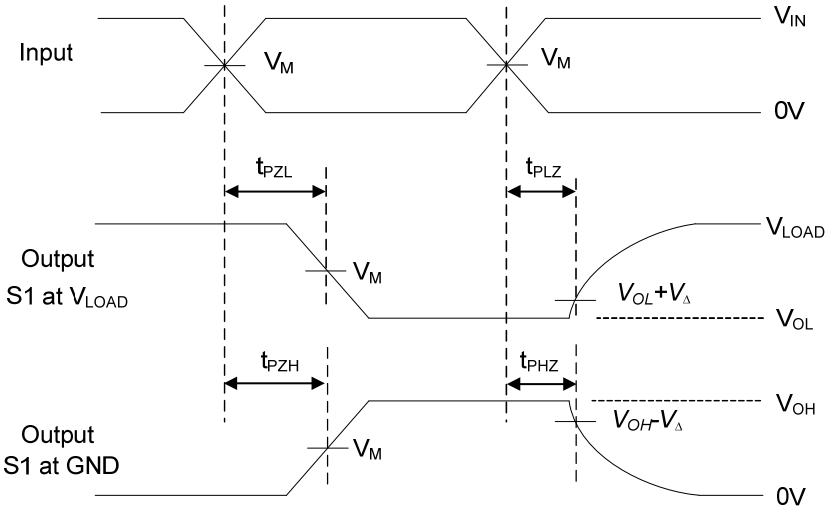


Setup and Hold Times

■ TEST CIRCUIT AND WAVEFORMS (Cont.)



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enble and Disable Times

Note: A. C_L includes probe and jig capacitance.

B. $P_{RR} \leqslant 1MHz$, $Z_O = 50\Omega$, $t_R \leqslant 3ns$, $t_F \leqslant 3ns$.