



U74AHCT3G34

CMOS IC

TRIPLE BUFFER GATE

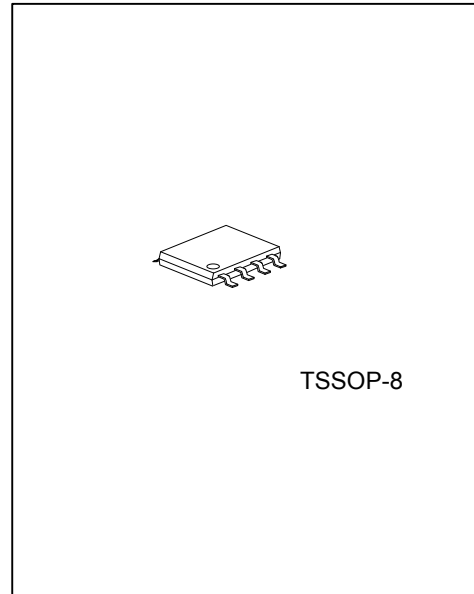
DESCRIPTION

The **U74AHCT3G34** is a high-speed Si-gate CMOS device which provides three buffers with the function $Y=A$.

The **U74AHCT3G34** is compatible of TTL input switching levels and has supply voltage range from 4.5V to 5.5V.

FEATURES

- * Low power supply 1.0 μ A at 5.5 V
- * Up to 5.5 V inputs accept voltages
- * Typical t_{PD} of 3.4ns at $V_{CC} = 5.0 V, C_L = 15 pF$
- * Low power dissipation
- * Symmetrical output impedance
- * Balanced propagation delays
- * High noise immunity

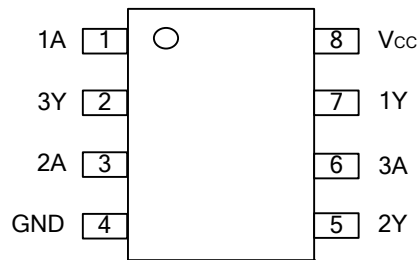


ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHCT3G34L-P08-R	U74AHCT3G34G-P08-R	TSSOP-8	Tape Reel
U74AHCT3G34L-P08-T	U74AHCT3G34G-P08-T	TSSOP-8	Tube

<p>U74AHCT3G34L-P08-R</p> <p>(1)Packing Type (2)Package Type (3)Lead Free</p>	<p>(1) R: Tape Reel, T: Tube (2) P08: TSSOP-8 (3) G:Halogen Free, L: Lead Free</p>
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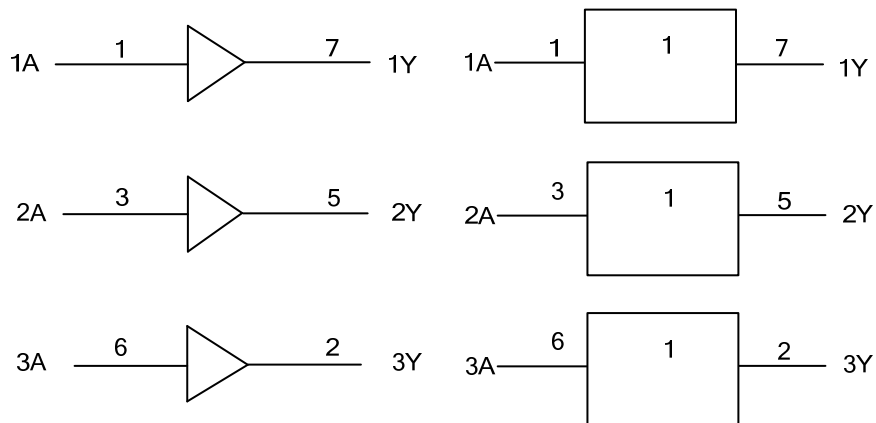
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT(A)	OUTPUT(Y)
L	L
H	H

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
Input Voltage	V_{IN}	-0.5 ~ 7.0	V
Output Voltage	V_{OUT}	-0.5 ~ $V_{CC} + 0.5$	V
V_{CC} or GND Current	I_{CC}	±75	mA
Output Current	I_{OUT}	±25	mA
Input Clamp Current	I_{IK}	-20	mA
Output Clamp Current	I_{OK}	±20	mA
Operating Temperature	T_{OPR}	-40 ~ + 125	°C
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Rise or Fall Times	t_R, t_F	$V_{CC} = 5.0 \pm 0.5V$			20	ns/V

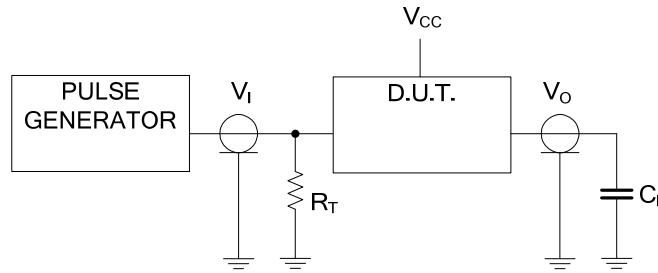
■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage	V_{IH}	$V_{CC} = 4.5$ to 5.5 V	2.0			V
Low-level input voltage	V_{IL}	$V_{CC} = 4.5$ to 5.5 V			0.8	V
High-Level Output Voltage	V_{OH}	$V_{CC} = 4.5V, V_I = V_{IH}$ or $V_{IL}, I_O = -50\mu A$	4.4	4.5		V
		$V_{CC} = 4.5V, V_I = V_{IH}$ or $V_{IL}, I_O = -8.0mA$	3.94	-		V
Low-Level Output Voltage	V_{OL}	$V_{CC} = 4.5V, V_I = V_{IH}$ or $V_{IL}, I_O = -50\mu A$		0	0.1	V
		$V_{CC} = 4.5V, V_I = V_{IH}$ or $V_{IL}, I_O = -8.0mA$			0.36	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC} = 5.5V, V_I = V_{IH}$ or V_{IL}			0.1	μA
Quiescent Supply Current	I_{CC}	$V_{CC} = 5.5V, V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$			1.0	μA
Additional Quiescent Supply Current per input pin	ΔI_{CC}	$V_{CC} = 5.5V$, One input at 3.4V, $I_{OUT} = 0$, Other inputs at V_{CC} or GND			1.35	mA
Input Capacitance	C_{IN}	$V_{IN} = V_{CC}$ or GND		1.5	10	pF

■ SWITCHING CHARACTERISTICS ($T_A=25^\circ C, t_R = t_F \leq 3$ ns, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Propagation delay from input (A) to output(Y)	t_{PLH}	$C_L = 15pF$	$V_{CC} = 4.5$ to 5.5 V			6.7	ns
			$V_{CC} = 5V$		3.4		ns
	t_{PHL}	$C_L = 50 pF$	$V_{CC} = 4.5$ to 5.5 V			7.7	ns
			$V_{CC} = 5V$		4.9		ns

■ TEST CIRCUIT AND WAVEFORMS

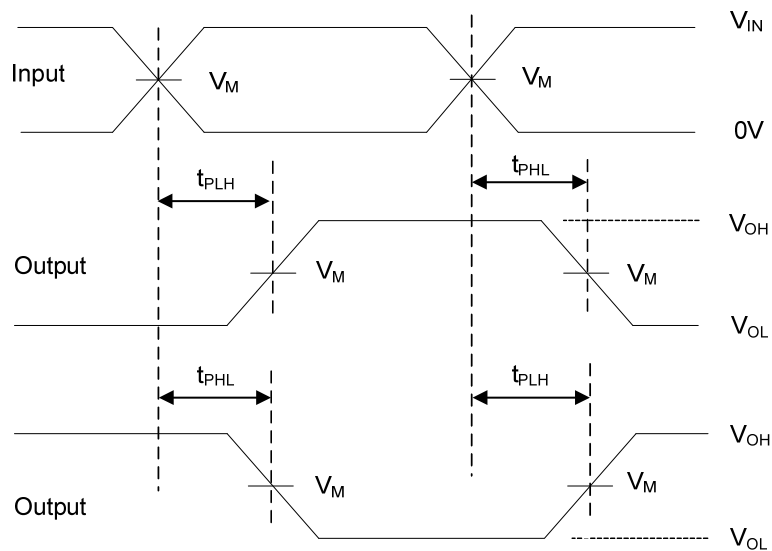


Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generator.

V_{CC}	Inputs		V_M	C_L
	V_{IN}	t_R, t_F		
4.5 to 5.5V	GND to 3.0 V	$\leq 3ns$	1.5 V	15 or 50 pF



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