



U74CBT2G125

CMOS IC

Dual Bus Switch with Level Shift

DESCRIPTION

The **U74CBT2G125** is a low on-resistance, high-speed CMOS 2-bit bus switch. This bus switch allows the connections or disconnections to be made with minimal propagation delay while maintaining Low power dissipation which is the feature of CMOS.

When output enable (\overline{OE}) is at low level, the switch is on; when at high level, the switch is off.

The device is enable to realize the shift of signal level from 5V to 3.3 V. All inputs are equipped with protector circuits to protect the device from static discharge.

FEATURES

- * Operating voltage: $V_{CC}=4.0\sim 5.5V$
- * High speed operation: $t_{PD}=0.32\text{ ns (max)}$
- * Ultra-low on resistance: $R_{ON}=5\Omega\text{ (typ.)}$
- * TTL level input (control input)
- * Low Power Dissipation: $I_{CC}=10\mu A\text{ (max.)}$

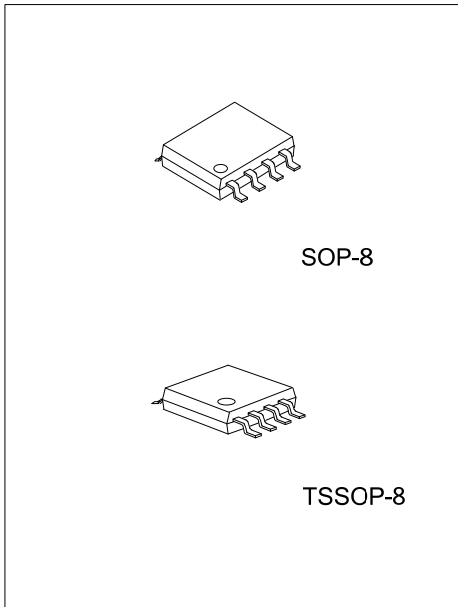
ORDERING INFORMATION

Ordering Number	Package	Packing
U74CBT2G125G-S08-R	SOP-8	Tape Reel
U74CBT2G125G-P08-R	TSSOP-8	Tape Reel

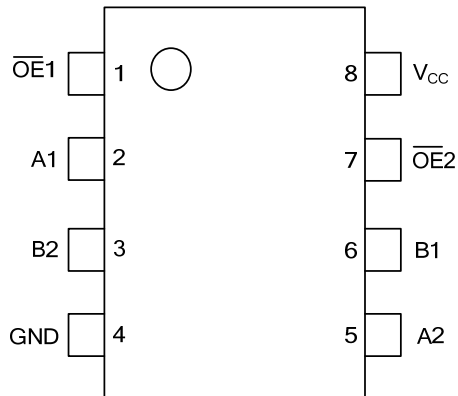
<p>U74CBT2G125G-S08-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) S08: SOP-8, P08: TSSOP-8 (3) G: Halogen Free and Lead Free</p>
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MARKING

SOP-8	TSSOP-8



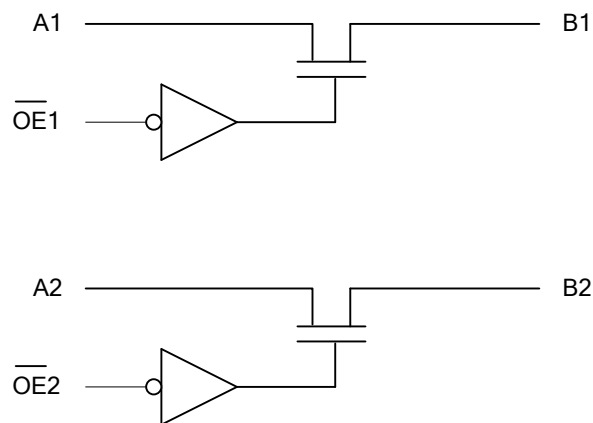
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT		OUTPUT
\overline{OE}		
L		A port = B port
H		Disconnect

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7.0	V
Input Voltage	V_{IN}	-0.5~7.0	V
Switch terminal I/O voltage	V_S	-0.5~7.0	V
Switch I/O current	I_S	128	mA
Input Clamp Current($V_I < 0$)	I_{IK}	-50	mA
DC VCC/GND current	I_{CC}/I_{GND}	± 100	mA
Storage Temperature	T_{STG}	-65 ~ +150	$^{\circ}C$

Note 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	97	$^{\circ}C/W$
	TSSOP-8	149	$^{\circ}C/W$

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	4		5.5	V
Control pin input voltage	V_{IN}	0		5.5	V
Switch I/O voltage	V_S	0		5.5	V
High-control input voltage	V_{IH}	2			V
Low-control input voltage	V_{IL}			0.8	V
Operating Temperature	T_A	-40		+85	$^{\circ}C$
Control pin input rise/fall time	dt/dv	0		10	ns/V

■ STATIC CHARACTERISTICS

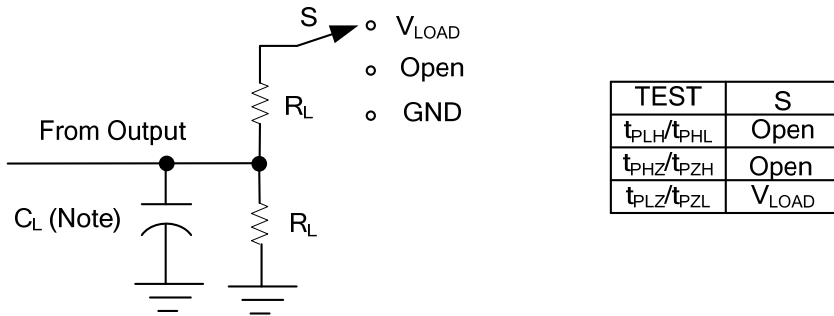
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Digital Input Diode Voltage	V_{IK}	$V_{CC}=4, I_i=-18mA$			-1.2	V	
High-level output voltage	V_{OH}	$V_{CC}=4.75V$	$I_{OH}=1\mu A, V_{IS}=V_{CC}$	2.3	2.8	3.2	V
		$V_{CC}=5.0V$		2.5	3.0	3.4	V
		$V_{CC}=5.25V$		2.7	3.2	3.6	V
Input leakage current	I_{IN}	$V_{CC}=4.5\sim 5.5V, V_{IN}=0\sim 5.5V$			± 1.0	μA	
Quiescent Supply Current	I_{CC}	$V_{CC}=5.5V, V_I=5.5V$ or GND, $I_O=0$			10	μA	
Additional Quiescent Supply Current	ΔI_{CC}	$V_{CC}=5.5V, V_{IN}=3.4V$ (one input)			2.5	mA	
Power off leakage current	I_{OFF}	$V_{CC}=0, A=B=\overline{OE}=0\sim 5.5V$			± 1.0	μA	
Off-STATE leakage current (switch off)	I_{SZ}	$V_{CC}=4.5\sim 5.5V, A,B=0\sim 5.5V, \overline{OE}=V_{CC}$			± 1.0	μA	
Control Input Capacitance	C_{IN}	$V_{CC}=5V$		3		pF	
Switch terminal capacitance	$C_{I/O}$	$V_{CC}=5V, \overline{OE}=V_{CC}$		10		pF	
ON-Resistance	R_{ON}	$V_{CC}=4.5V$	$V_I=0V$	$I_I=64mA$	5	9	Ω
				$I_I=30mA$	5	9	Ω
		$V_{CC}=4.75V$	$V_I=0V$	$I_I=64mA$	5	8	Ω
				$I_I=30mA$	5	8	Ω
			$V_I=2.3V, I_I=-15mA$		35	65	Ω
					35	50	Ω

■ DYNAMIC CHARACTERISTICS (Input: $t_R, t_F \leq 2.5\text{ns}$; $\text{PRR} \leq 10\text{MHz}$; $C_L = 50\text{pF}$)

See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From input (A or B) to output (B or A)	t_{pd}	$V_{CC} = 4.5\text{V}$			0.32	ns
From input \overline{OE} to output (A or B)	t_{en}	$V_{CC} = 4.5\text{V}$			4.5	ns
From input \overline{OE} to output (A or B)	t_{dis}	$V_{CC} = 4.5\text{V}$			5.0	ns

■ TEST CIRCUIT AND WAVEFORMS (CL=50pF, RL=500Ω, VLOAD=7V, VM=1.5V)



Note: CL includes probe and jig capacitance.

Fig. 1 Load circuitry for switching times

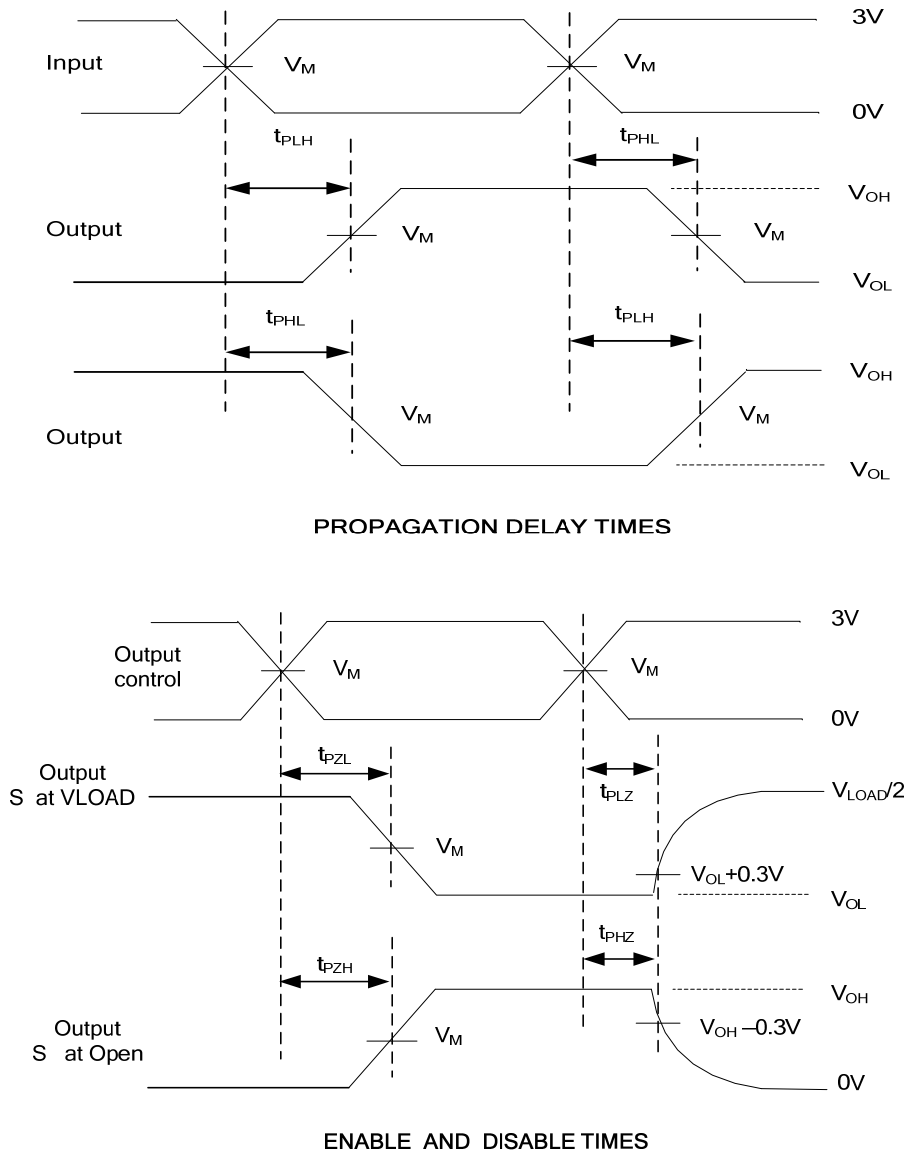


Fig. 2 Propagation delay from input(A) to output(B) and Output transition time

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