



## U74CBT3306

CMOS IC

### DUAL FET BUS SWITCH

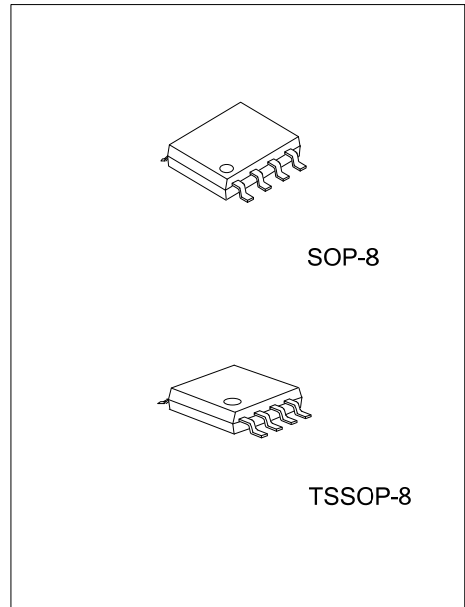
#### DESCRIPTION

The **U74CBT3306** dual FET bus switch features independent line switches.

Each switch is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

#### FEATURES

- \* 5- $\Omega$  Switch Connection Between Two Ports
- \* TTL-Compatible Input Levels



#### ORDERING INFORMATION

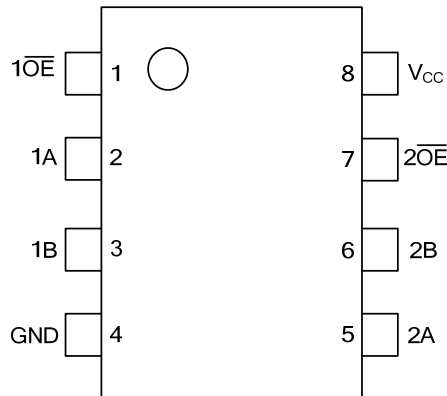
Ordering Number	Package	Packing
U74CBT3306G-S08-R	SOP-8	Tape Reel
U74CBT3306G-P08-R	TSSOP-8	Tape Reel

<p>U74CBT3306G-S08-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) S08: SOP-8, P08: TSSOP-8 (3) G: Halogen Free and Lead Free</p>
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#### MARKING

SOP-8	TSSOP-8
<p>8 7 6 5 → Date Code UTC □□□□ CBT3306G □□ → Lot Code 1 2 3 4</p>	<p>8 7 6 5 → Date Code UTC □□□□ C306G □□ → Lot Code 1 2 3 4</p>

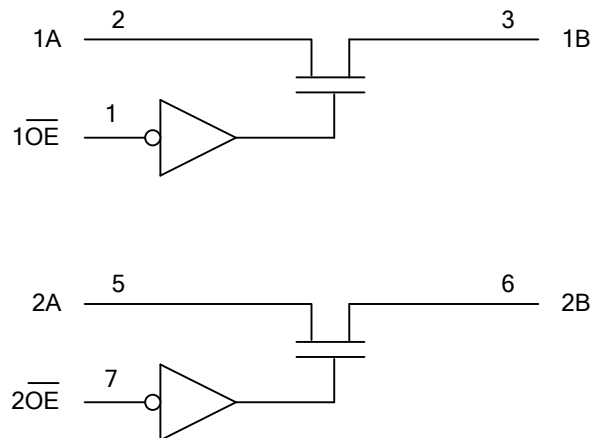
■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUT	FUNCTION
$\overline{OE}$	
L	A port = B port
H	Disconnect

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T<sub>A</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V <sub>CC</sub>	-0.5 ~ 7	V
Input Voltage range(see Note 1)	V <sub>IN</sub>	-0.5 ~ 7	V
Input Clamp Current	I <sub>IK</sub>	-50	mA
Continuous channel current		128	mA
Storage Temperature range	T <sub>STG</sub>	-65~+150	°C

Notes: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	SOP-8	97	°C/W
	TSSOP-8	149	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V <sub>CC</sub>	4		5.5	V
High-Level Control Input Voltage	V <sub>IH</sub>	2			V
Low-Level Control Input Voltage	V <sub>IL</sub>			0.8	V
Operating Temperature	T <sub>A</sub>	-40		85	°C

■ ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C, unless otherwise specified)

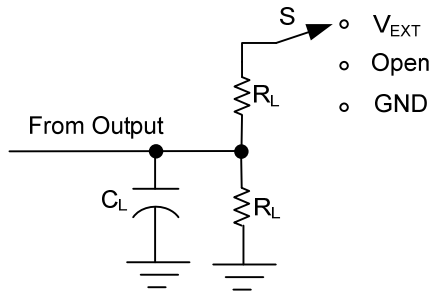
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Control Input Clamp Voltage	V <sub>IK</sub>	V <sub>CC</sub> =4.5V, I <sub>IN</sub> =-18mA			-1.2	V	
Input Leakage Current	I <sub>I(LEAK)</sub>	V <sub>CC</sub> =5.5V, V <sub>IN</sub> =V <sub>CC</sub> or GND			±1	µA	
Quiescent Supply Current	I <sub>CC</sub>	V <sub>CC</sub> =5.5V, I <sub>OUT</sub> =0, V <sub>IN</sub> =V <sub>CC</sub> or GND			3	µA	
Additional Quiescent Supply Current	ΔI <sub>CC</sub>	V <sub>CC</sub> =5.5V, One input at 3.4V, Other inputs at V <sub>CC</sub> or GND			2.5	mA	
Control Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =3V or 0		3		pF	
Input Capacitance	C <sub>IO(OFF)</sub>	V <sub>OUT</sub> =3V or 0, $\overline{OE}$ =V <sub>CC</sub>		4		pF	
ON-Resistance	R <sub>ON</sub>	V <sub>CC</sub> =4V, V <sub>IN</sub> =2.4V, I <sub>OUT</sub> =-15mA		14	20	Ω	
		V <sub>CC</sub> =4.5V, V <sub>IN</sub> =0		5	7	Ω	
			I <sub>OUT</sub> =64mA		5	7	Ω
			I <sub>OUT</sub> =30mA		5	7	Ω
		V <sub>CC</sub> =4.5V, V <sub>IN</sub> =2.4V		10	15	Ω	

■ SWITCHING CHARACTERISTICS (C<sub>L</sub>=50pF, R<sub>L</sub>=500Ω. see TEST CIRCUIT AND WAVEFORMS)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From input (A or B) to output (B or A) (Note)	t <sub>pd</sub>	V <sub>CC</sub> =4V			0.35	ns
		V <sub>CC</sub> =5V±0.5V			0.25	ns
From input $\overline{OE}$ to output (A or B)	t <sub>en</sub>	V <sub>CC</sub> =4V			5.6	ns
		V <sub>CC</sub> =5V±0.5V	1.8		5	ns
From input $\overline{OE}$ to output (A or B)	t <sub>dis</sub>	V <sub>CC</sub> =4V			4.6	ns
		V <sub>CC</sub> =5V±0.5V	1		4.3	ns

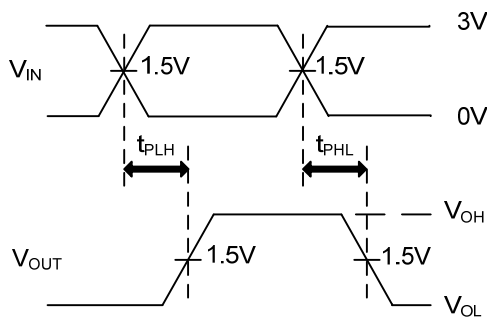
Note: The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## TEST CIRCUIT AND WAVEFORMS

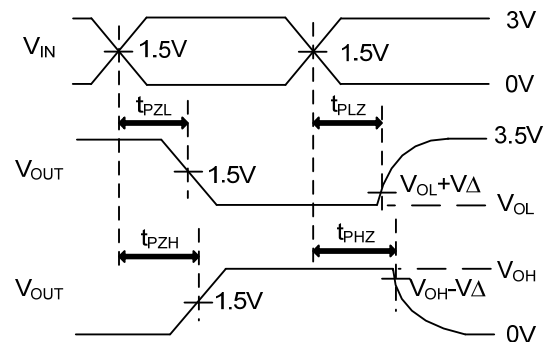


TEST	S
$t_{PLH}/t_{PHL}$	Open
$t_{PHZ}/t_{PZH}$	Open
$t_{PLZ}/t_{PZL}$	$V_{EXT}$

TEST	$V_{CC}$	$V_i$	$t_r / t_f$	$V_{\Delta}$	$V_{EXT}$	$C_L$	$R_L$
$t_{PLH}/t_{PHL}$	4V	$V_{CC}$ or GND	$\leq 2.5$ ns		Open	50pF	500 $\Omega$
	$5V \pm 0.5V$	$V_{CC}$ or GND	$\leq 2.5$ ns		Open	50pF	500 $\Omega$
$t_{PLZ}/t_{PZL}$	4V	GND	$\leq 2.5$ ns	0.3V	7V	50pF	500 $\Omega$
	$5V \pm 0.5V$	GND	$\leq 2.5$ ns	0.3V	7V	50pF	500 $\Omega$
$t_{PHZ}/t_{PZH}$	4V	$V_{CC}$	$\leq 2.5$ ns	0.3V	Open	50pF	500 $\Omega$
	$5V \pm 0.5V$	$V_{CC}$	$\leq 2.5$ ns	0.3V	Open	50pF	500 $\Omega$



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

- Notes:
- $C_L$  includes probe and jig capacitance.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$ MHz,  $Z_0 = 50\Omega$ ,  $t_r \leq 2.5$ ns,  $t_f \leq 2.5$ ns.
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}(s)$ .
  - All parameters and waveforms are not applicable to all devices.

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