



U74HC540

CMOS IC

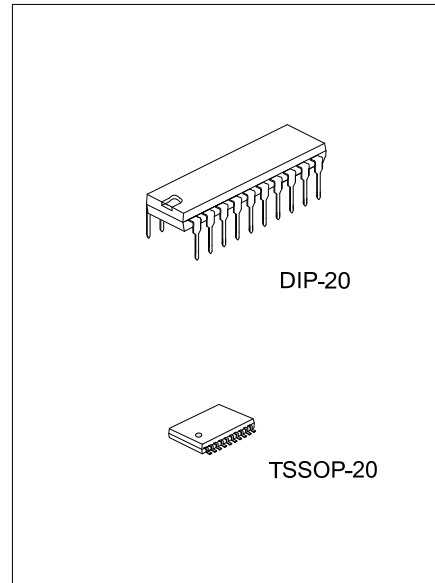
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

DESCRIPTION

The **U74HC540** combines with octal buffers and line drivers with inverting 3-state outputs. The 3-state output is controlled by output enable inputs $\overline{OE1}$ and $\overline{OE2}$, all eight outputs will be in high-impedance when either of the 2 inputs is applied with high voltage.

FEATURES

- * Operation voltage range: 2V ~ 6V
- * High-current 3-state outputs for bus driver
- * Inverting outputs



ORDERING INFORMATION

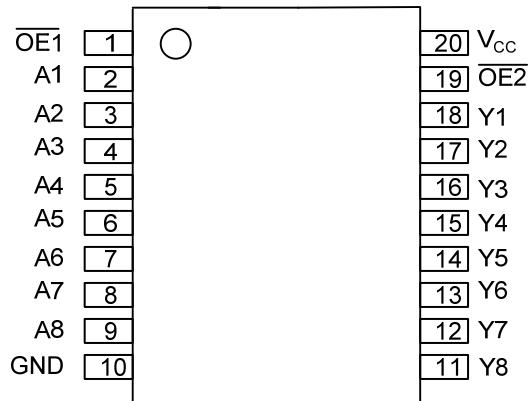
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC540L-D20-T	U74HC540G-D20-T	DIP-20	Tube
-	U74HC540G-P20-R	TSSOP-20	Tape Reel

<p>U74HC540L-D20-T</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) D20: DIP-20, P20: TSSOP-20</p> <p>(3) L: Lead Free, G: Halogen Free and Lead Free</p>
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MARKING

DIP-20	TSSOP-20
<p>Date Code</p> <p>UTC □□□□</p> <p>L: Lead Free</p> <p>U74HC540 □</p> <p>G: Halogen Free</p> <p>Lot Code</p>	<p>Date Code</p> <p>UTC □□□□</p> <p>U74HC540G</p> <p>Lot Code</p>

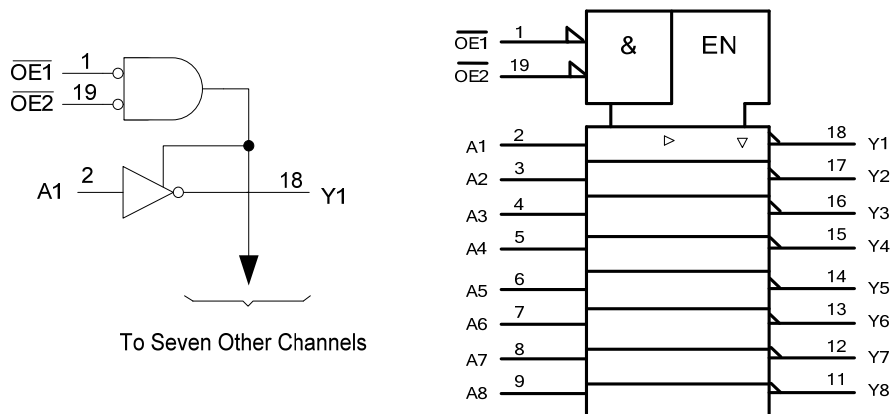
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATINGS (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7	V
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Output Current	I_{OUT}	±35	mA
V_{CC} or GND Current	I_{CC}	±70	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2	5	6	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	t_R, t_F	$V_{CC}=2V$	0		1000	ns
		$V_{CC}=4.5V$	0		500	
		$V_{CC}=6V$	0		400	
Operating Temperature	T_A		-40		85	°C

■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC}=2V$	1.5			V
		$V_{CC}=4.5V$	3.15			
		$V_{CC}=6V$	4.2			
Low-Level Input Voltage	V_{IL}	$V_{CC}=2V$			0.5	V
		$V_{CC}=4.5V$			1.35	
		$V_{CC}=6V$			1.8	
High-Level Output Voltage	V_{OH}	$V_{CC}=2V, I_{OH}=-20\mu A$	1.9	1.998		V
		$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4	4.499		
		$V_{CC}=6V, I_{OH}=-20\mu A$	5.9	5.999		
		$V_{CC}=4.5V, I_{OH}=-6mA$	3.98	4.3		
		$V_{CC}=6V, I_{OH}=-7.8mA$	5.48	5.8		
Low-Level Output Voltage	V_{OL}	$V_{CC}=2V, I_{OH}=20\mu A$		0.002	0.1	V
		$V_{CC}=4.5V, I_{OH}=20\mu A$		0.001	0.1	
		$V_{CC}=6V, I_{OH}=20\mu A$		0.001	0.1	
		$V_{CC}=4.5V, I_{OL}=6mA$		0.17	0.26	
		$V_{CC}=6V, I_{OL}=7.8mA$		0.15	0.26	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=6V, V_{IN}=V_{CC}$ or GND		±0.1	±100	nA
Output Leakage Current	$I_{O(LEAK)}$	$V_{CC}=6V, V_{OUT}=V_{CC}$ or GND		±0.01	±0.5	uA
Quiescent Supply Current	I_Q	$V_{CC}=6V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			8	μA
Input Capacitance	C_{IN}	$V_{CC}=2V\sim 6V$		3	10	pF
Propagation delay from input (A) to output(Y)	t_{PLH}/ t_{PHL}	$V_{CC}=2V, C_L=50 pF$		35	100	ns
		$V_{CC}=2V, C_L=150 pF$		60	150	
		$V_{CC}=4.5V, C_L=50 pF$		10	20	
		$V_{CC}=4.5V, C_L=150 pF$		15	30	
		$V_{CC}=6V, C_L=50 pF$		8	17	
		$V_{CC}=6V, C_L=150 pF$		13	26	

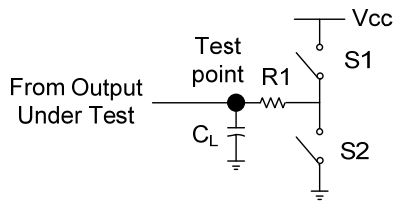
■ SWITCHING CHARACTERISTICS ($t_R, t_F \leq 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
3-state output enable time from $\overline{\text{OE}}$ to Y_n	t_{PZH}/ t_{PZL}	$V_{CC}=2\text{V}, C_L=50\text{ pF}$		75	150	ns
		$V_{CC}=2\text{V}, C_L=150\text{ pF}$		100	200	
		$V_{CC}=4.5\text{V}, C_L=50\text{ pF}$		15	30	
		$V_{CC}=4.5\text{V}, C_L=150\text{ pF}$		20	40	
		$V_{CC}=6\text{V}, C_L=50\text{ pF}$		13	26	
		$V_{CC}=6\text{V}, C_L=150\text{ pF}$		17	34	
3-state output disable time from $\overline{\text{OE}}$ to Y_n	t_{PHZ}/ t_{PLZ}	$V_{CC}=2\text{V}, C_L=50\text{ pF}$		40	150	ns
		$V_{CC}=4.5\text{V}, C_L=50\text{ pF}$		18	30	
		$V_{CC}=6\text{V}, C_L=50\text{ pF}$		17	26	

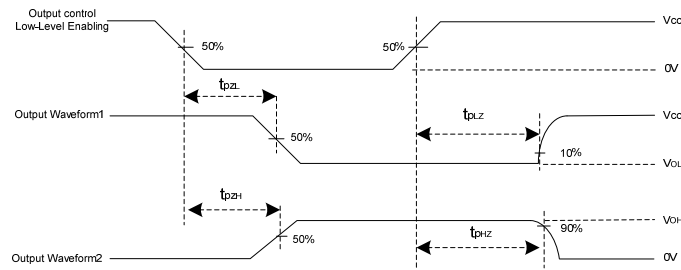
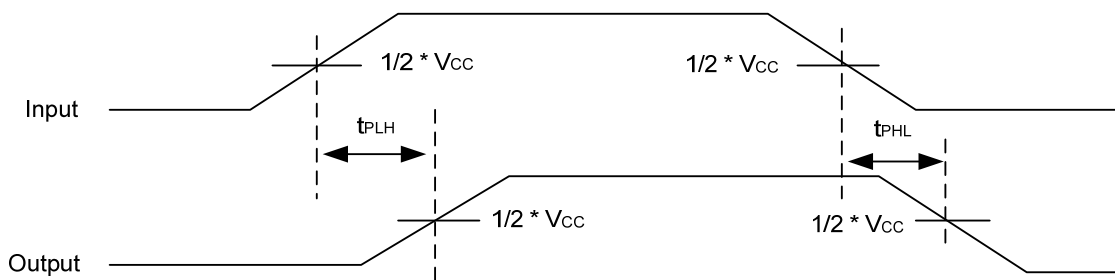
■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Cpd	No load, $f=1\text{MHz}$		35		pF

■ TEST CIRCUIT AND WAVEFORMS



Note: C_L includes probe and jig capacitance.



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