



U74HC594

CMOS IC

8-BIT SERIAL-IN SHIFT REGISTER WITH OUTPUT REGISTERS

DESCRIPTION

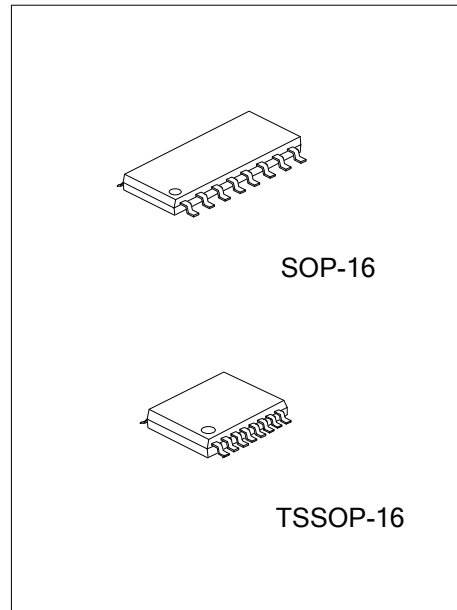
The UTC **U74HC594** contains an 8-bit serial-in parallel-out register. The Serial Data Input (SER) input will shift into the internal shift register during every LOW-to-HIGH transition on the ($\overline{\text{SRCLR}}$) input. The storage register will storage the 8-bit data from the shift register during the LOW-to-HIGH transition on the ($\overline{\text{RCLR}}$) input. A serial (QH') output is provided for cascading purposes.

FEATURES

- * Wide supply voltage range from 2.0V to 6.0V
- * Low static power consumption; $I_{CC}=8\mu\text{A}$ (Max.)
- * 8 bit counter with register

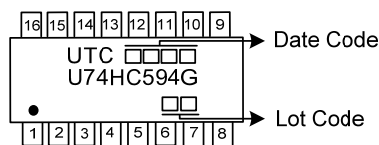
ORDERING INFORMATION

Ordering Number	Package	Packing
U74HC594G-S16-R	SOP-16	Tape Reel
U74HC594G-P16-R	TSSOP-16	Tape Reel

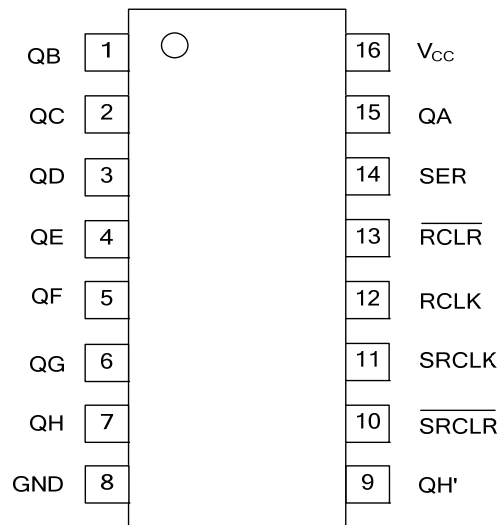


<p>U74HC594G-S16-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) S16: SOP-16, P16: TSSOP-16</p> <p>(3) G: Halogen Free and Lead Free</p>
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MARKING



■ PIN CONFIGURATION

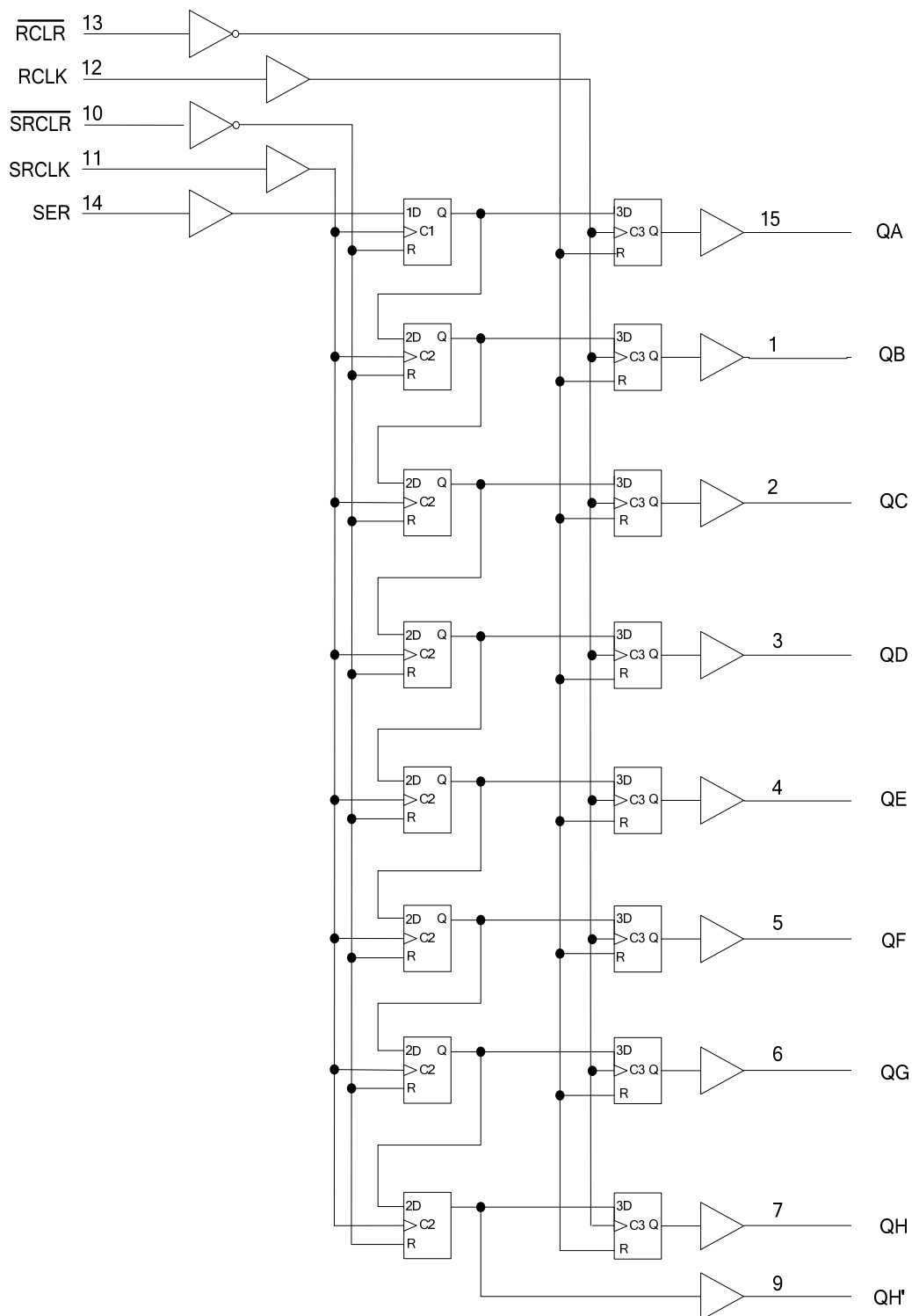


■ FUNCTION TABLE

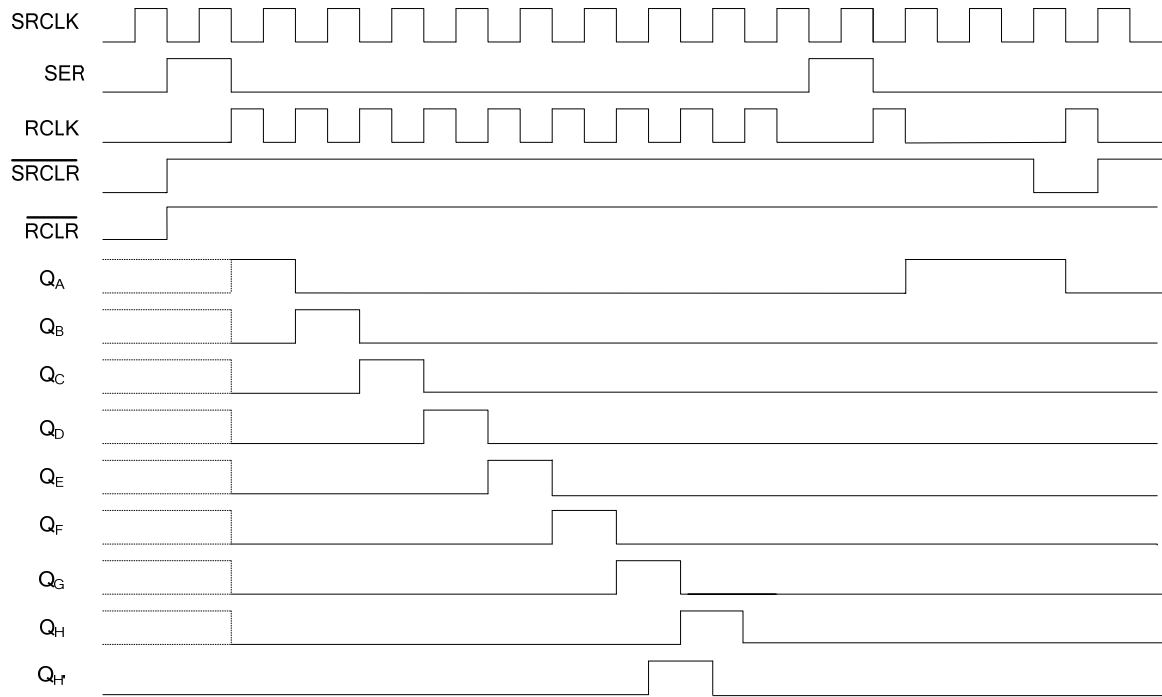
INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	RCLR	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift-register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

Note: L: low voltage level; H: high voltage level; ↑: low-to-high; X: don't care

■ LOGIC DIAGRAM (positive logic)



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Continuous V_{CC} or GND Current	I_{CC}		±75	µA
Continuous Output Current	I_{OUT}	$V_{OUT}=0V \sim V_{CC}$	±35	mA
Input Clamp Current	I_{IK}	$V_{IN}<0V$ or $V_{IN}>V_{CC}$	±20	mA
Output Clamp Current	I_{OK}	$V_{OUT}>V_{CC}$ or $V_{OUT}<0V$	±20	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0		6.0	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=2.0V$			1000	ns
		$V_{CC}=4.5V$			500	ns
		$V_{CC}=6.0V$			400	ns
Operating Temperature	T_A		-40		+85	°C

■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	$V_{CC}=2.0V$	1.5			V
		$V_{CC}=4.5V$	3.15			V
		$V_{CC}=6.0V$	4.2			V
Low-level Input Voltage	V_{IL}	$V_{CC}=2.0V$			0.5	V
		$V_{CC}=4.5V$			1.35	V
		$V_{CC}=6.0V$			1.8	V
High-Level Output Voltage	V_{OH}	$V_{CC}=2.0V, I_{OH}=-20\mu A$	1.9	1.998		V
		$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4	4.499		V
		$V_{CC}=6.0V, I_{OH}=-20\mu A$	5.9	5.999		V
		$V_{CC}=4.5V, I_{OH}=-6mA$	3.98			V
		$V_{CC}=6V, I_{OH}=-7.8mA$	5.48			V
Low-Level Output Voltage	V_{OL}	$V_{CC}=2.0V, I_{OL}=20\mu A$		0.002	0.1	V
		$V_{CC}=4.5V, I_{OL}=20\mu A$		0.001	0.1	V
		$V_{CC}=6.0V, I_{OL}=20\mu A$		0.001	0.1	V
		$V_{CC}=4.5V, I_{OL}=6mA$			0.26	V
		$V_{CC}=6.0V, I_{OL}=7.8mA$			0.26	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=6.0V, V_{IN}=V_{CC}$ or GND			±0.1	µA
3-state Output OFF-state Current	I_{OZ}	$V_{IN}=V_{IH}$ or $V_{IL}, V_{OUT}=V_{CC}$ or GND, $V_{CC}=6.0V$			±0.5	µA
Quiescent Supply Current	I_{CC}	$V_{CC}=6.0V, V_{IN}=V_{CC}$ or 0V, $I_{OUT}=0A$			8	µA
Input Capacitance	C_I	$V_{CC}=6.0V, V_{IN}=V_{CC}$ or GND		3	10	pF

■ SWITCHING CHARACTERISTICS (C_L=50pF, T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Maximum clock pulse frequency	f _{MAX}	C _L =50pF	V _{CC} =2.0V	5	8		MHz
			V _{CC} =4.5V	25	35		MHz
			V _{CC} =6.0V	29	40		MHz
Propagation delay from input (SRCLK) to output (QH')	t _{PD}	C _L =50pF	V _{CC} =2.0V		50	150	ns
			V _{CC} =4.5V		20	30	ns
			V _{CC} =6.0V		15	25	ns
Propagation delay from input (RCLK) to output (Q _A -Q _H)		C _L =50pF	V _{CC} =2.0V		50	150	ns
			V _{CC} =4.5V		20	30	ns
			V _{CC} =6.0V		15	25	ns
	C _L =150pF	V _{CC} =2.0V		90	200	ns	
		V _{CC} =4.5V		23	40	ns	
		V _{CC} =6.0V		19	34	ns	
Propagation delay from input (SRCLK) to output (QH')	t _{PHL}	C _L =50pF	V _{CC} =2.0V		50	150	ns
			V _{CC} =4.5V		20	30	ns
			V _{CC} =6.0V		15	25	ns
Propagation delay from input (RCLR) to output (Q _A -Q _H)		C _L =50pF	V _{CC} =2.0V		50	125	ns
			V _{CC} =4.5V		20	25	ns
			V _{CC} =6.0V		15	21	ns
	C _L =150pF	V _{CC} =2.0V		90	200	ns	
		V _{CC} =4.5V		23	40	ns	
		V _{CC} =6.0V		19	34	ns	
Propagation delay to output (QH')	t _t	C _L =50pF	V _{CC} =2.0V		38	75	ns
			V _{CC} =4.5V		8	15	ns
			V _{CC} =6.0V		6	13	ns
Propagation delay to output (Q _A -Q _H)		C _L =50pF	V _{CC} =2.0V		38	60	ns
			V _{CC} =4.5V		8	12	ns
			V _{CC} =6.0V		6	10	ns
	C _L =150pF	V _{CC} =2.0V		45	210	ns	
		V _{CC} =4.5V		17	42	ns	
		V _{CC} =6.0V		13	36	ns	

■ TIMING REQUIREMENTS ($T_A=25^\circ\text{C}$, unless otherwise specified)

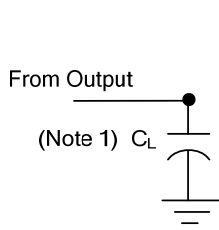
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Frequency	f_{CLOCK}	$V_{\text{CC}}=2.0\text{V}$			5	MHz
		$V_{\text{CC}}=4.5\text{V}$			25	MHz
		$V_{\text{CC}}=6.0\text{V}$			29	MHz
Pulse duration, SRCLK or RCLK high or low	t_w	$V_{\text{CC}}=2.0\text{V}$	100			ns
		$V_{\text{CC}}=4.5\text{V}$	20			ns
		$V_{\text{CC}}=6.0\text{V}$	17			ns
Pulse duration, $\overline{\text{SRCLK}}$ or $\overline{\text{RCLR}}$ Low	t_w	$V_{\text{CC}}=2.0\text{V}$	100			ns
		$V_{\text{CC}}=4.5\text{V}$	20			ns
		$V_{\text{CC}}=6.0\text{V}$	17			ns
Setup Time Before CLK \uparrow , SER before SRCLK \uparrow	t_{SU}	$V_{\text{CC}}=2.0\text{V}$	90			ns
		$V_{\text{CC}}=4.5\text{V}$	18			ns
		$V_{\text{CC}}=6.0\text{V}$	15			ns
Setup Time Before CLK \uparrow SRCLK \uparrow before RCLK \uparrow (Note)	t_{SU}	$V_{\text{CC}}=2.0\text{V}$	90			ns
		$V_{\text{CC}}=4.5\text{V}$	18			ns
		$V_{\text{CC}}=6.0\text{V}$	15			ns
Setup Time Before CLK \uparrow $\overline{\text{SRCLK}}$ low before RCLK \uparrow	t_{SU}	$V_{\text{CC}}=2.0\text{V}$	50			ns
		$V_{\text{CC}}=4.5\text{V}$	10			ns
		$V_{\text{CC}}=6.0\text{V}$	9			ns
Setup Time Before CLK \uparrow SRCLK high (inactive) before SRCLK \uparrow	t_{SU}	$V_{\text{CC}}=2.0\text{V}$	20			ns
		$V_{\text{CC}}=4.5\text{V}$	10			ns
		$V_{\text{CC}}=6.0\text{V}$	10			ns
Setup Time Before CLK \uparrow $\overline{\text{RCLR}}$ high (inactive) before SRCLK \uparrow	t_{SU}	$V_{\text{CC}}=2.0\text{V}$	5			ns
		$V_{\text{CC}}=4.5\text{V}$	5			ns
		$V_{\text{CC}}=6.0\text{V}$	5			ns
Setup Time Before CLK \uparrow Hold time, SER after SRCLK \uparrow	t_{H}	$V_{\text{CC}}=2.0\text{V}$	5			ns
		$V_{\text{CC}}=4.5\text{V}$	5			ns
		$V_{\text{CC}}=6.0\text{V}$	5			ns

Note: This setup time ensures that the output register receives stable data from the shift-register outputs. The clocks may be tied together, in which case the output register is one clock pulse behind the shift register.

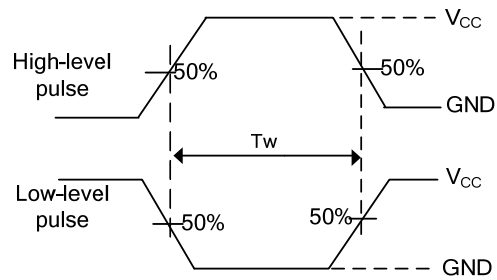
■ OPERATING CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load.		395		pF

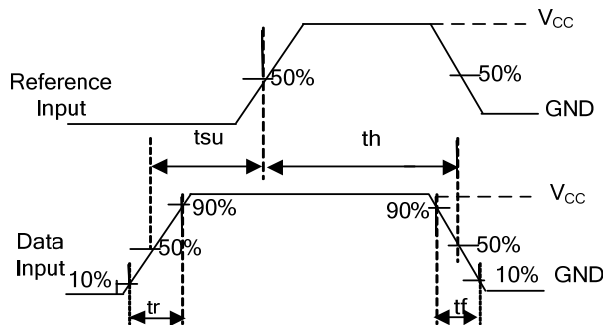
■ TEST CIRCUIT AND WAVEFORMS



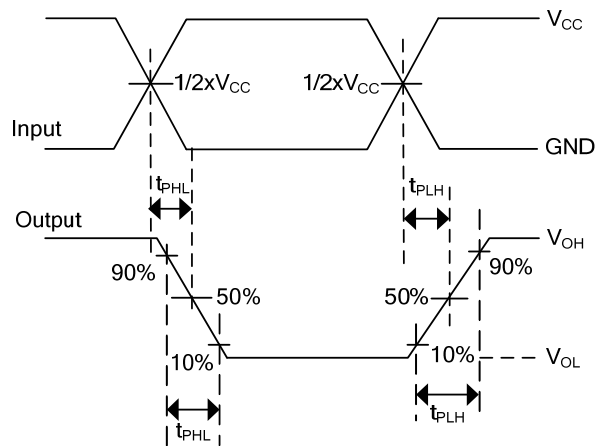
TEST CIRCUIT



PULSE WIDTH



SETUP TIME AND HOLD TIME



PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

Notes: 1. C_L includes probe and jig capacitance. $C_L=50\text{pF}$, $R_L=1\text{K}\Omega$.

2. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{MHz}$, $Z_O = 50\Omega$.

3. The outputs are measured one at a time, with one input transition per measurement.

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