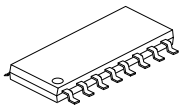
U74HCT4040

CMOS IC

12-BIT ASYNCHRONOUS BINARY COUNTERS



SOP-16

■ DESCRIPTION

The **U74HC4040** is a 12-stage asynchronous binary counter with a clock input (CLK), an overriding asynchronous master reset input (CLR) and twelve parallel outputs (Q0 to Q11). The counter advances on the High to Low transition of CLK. A HIGH on CLR clears all counter stages and forces all outputs Low, independent of the state of CLK. Each counter stage is a static toggle flip-flop. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

■ FEATURES

* Wide Operating Voltage Range of 4.5V to 5.5V
* Low Power Consumption, 8μA Maximum I_{CC}
* ±4mA Output Drive at 5V

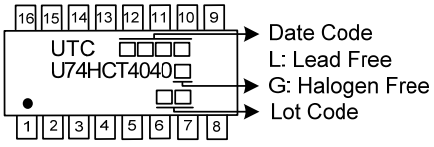
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT4040L-S16-R	U74HCT4040G-S16-R	SOP-16	Tape Reel

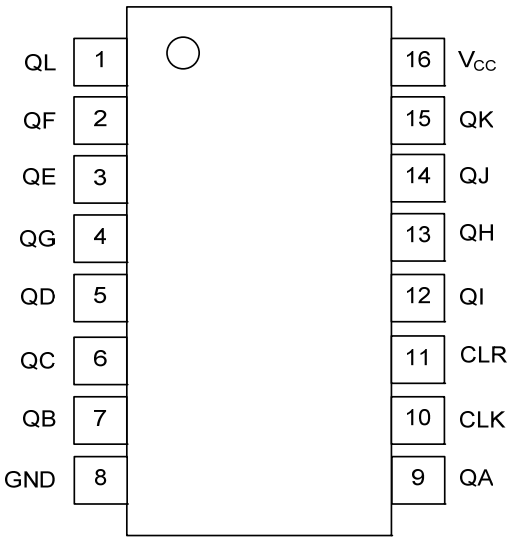
U74HCT4040G-S16-R
- (1)Packing Type
- (2)Package Type
- (3)Green Package

(1) R: Tape Reel
(2) S16: SOP-16
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

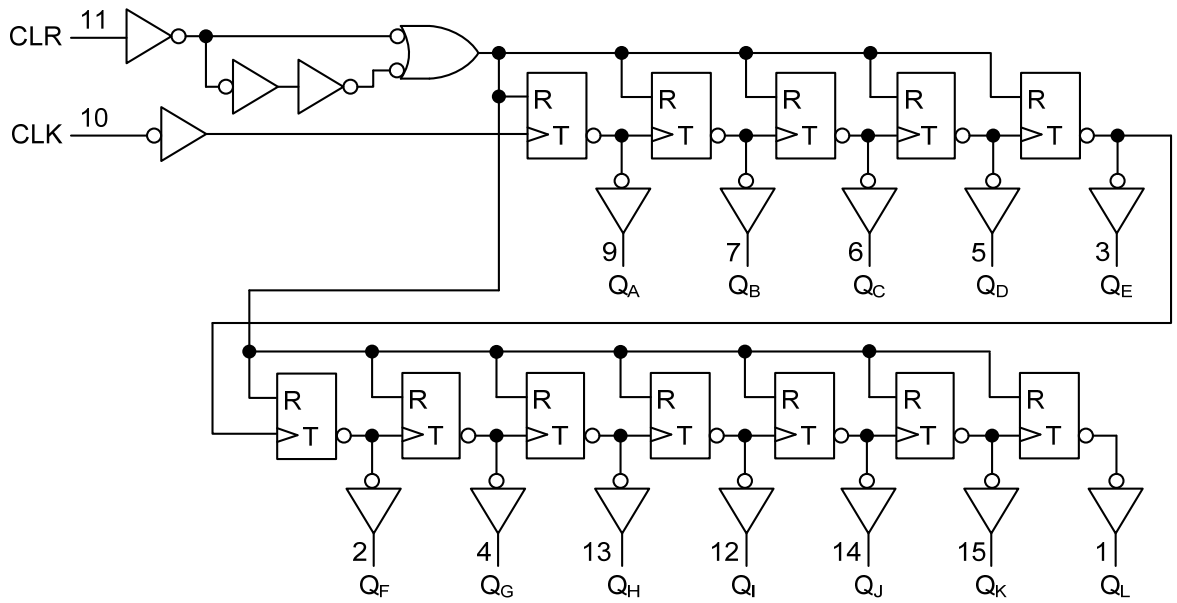


■ FUNCTION TABLE

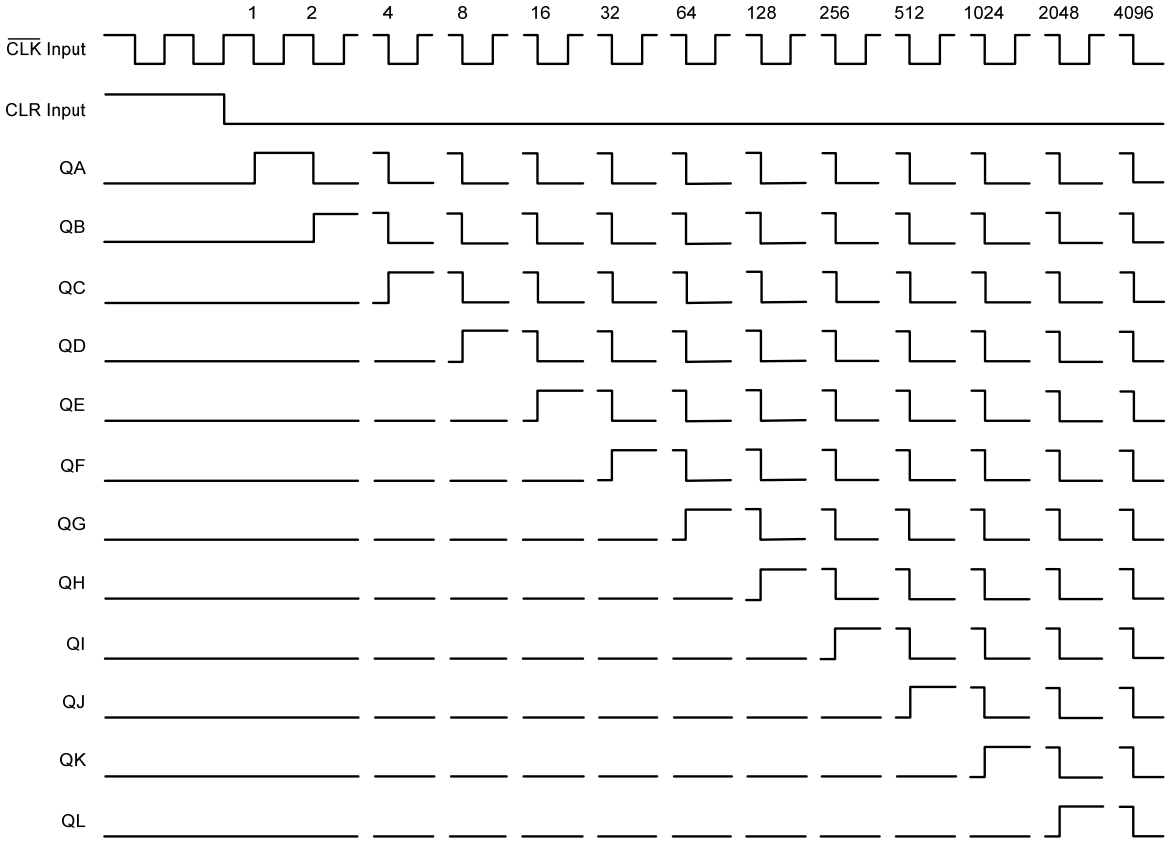
INPUTS		FUNCTION
CLK	CLR	Q0 to Q11
↑	L	No Change
↓	L	Advance to next stage
X	H	All Outputs L

Note: H = HIGH voltage level, L = LOW voltage level, X = don't care
↑ = LOW-to-HIGH clock transition, ↓ = HIGH-to-LOW clock transition.

■ LOGIC DIAGRAM (positive logic)



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Note 2)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Input Voltage	V_{IN}		-0.5 ~ V_{CC}+0.5	V
Output Voltage	V_{OUT}	Active Mode	-0.5 ~ V_{CC}+0.5	V
Continuous V_{CC} or GND Current	I_{CC}		±50	mA
Continuous Output Current	I_{OUT}	V_{OUT}=0V ~ V_{CC}	±25	mA
Input Clamp Current	I_{IK}	V_{IN}<0V or V_{IN}>V_{CC}	±20	mA
Output Clamp Current	I_{OK}	V_{OUT}>V_{CC} or V_{OUT}<0V	±20	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		+85	°C
Input Transition Rise or Fall Rate	Δt/Δt v	V_{CC}=4.5V			500	ns

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=4.5V~5.5V		2.0			V
Low-level Input Voltage	V_{IL}	V_{CC}=4.5V~5.5V				0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}, V_{CC}=4.5V	I_{OH}=-20μA	4.4			V
			I_{OH}=-4.0mA	3.98			V
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}, V_{CC}=4.5V	I_{OL}=20μA			0.1	V
			I_{OL}=4.0mA			0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=5.5V, V_{IN}= V_{CC} or GND			±0.01	±0.1	μA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0A				8	μA
Additional Quiescent Device Current Per Input Pin	$ΔI_{CC}$	V_{CC}=4.5V~5.5V, I_{OUT}=0A One input=V_{CC}-2.1V, other inputs at V_{CC} or GND				360	μA
Input Capacitance	C_I	V_{CC}=4.5V~5.5V, V_{IN}=V_{CC} or GND			3.5		pF

■ SWITCHING CHARACTERISTICS (T_A =25°C , t_R, t_F≤6nS ,unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Clock Pulse Frequency From Input (CLK)	f_{MAX}	V_{CC}=5V, C_L=15pF	25			MHz
Propagation Delay From Input (CLK) to Output (Q0)	t_{PHL}	V_{CC}=4.5V, C_L=50pF		19	40	ns
	t_{PLH}	V_{CC}=5.0V, C_L=15pF		17		
Propagation Delay From Input (Qn) to Output (Qn+1)	t_{PHL}	V_{CC}=4.5V, C_L=50pF		10	20	ns
	t_{PLH}	V_{CC}=5.0V, C_L=15pF		8		
Propagation Delay From Input (CLR) to Output (Qn)	t_{PHL}	V_{CC}=4.5V, C_L=50pF		23	45	ns

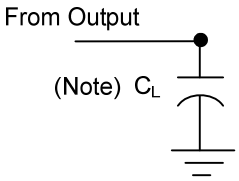
■ TIMING REQUIREMENTS (Input: t_R, t_F≤6nS; PRR≤1MHz)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Pulse Width High or Low (CLK)	t_W	V_{CC}=4.5V, C_L=50pF	16	7		ns
Reset Pulse Width High (CLR)		V_{CC}=4.5V, C_L=50pF	16	6		ns
Recovery Time (CLR) to (CLK)	t_{SU}	V_{CC}=4.5V, C_L=50pF	10	2		ns

■ OPERATING CHARACTERISTICS (T_A =25°C , unless otherwise specified)

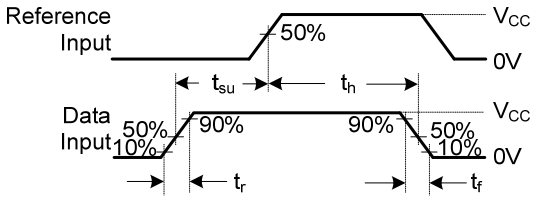
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}			20		pF

■ TEST CIRCUIT AND WAVEFORMS

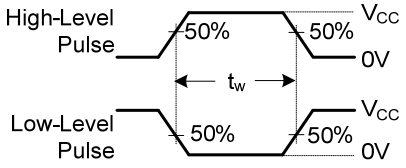


Note: C_L includes probe and jig capacitance. C_L=50pF, R_L=1KΩ.

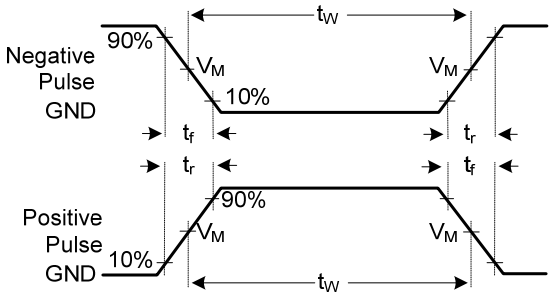
INPUT		LOAD	TEST
V_{IN}	t_r, t_f	C_L	
V_{CC}	6.0ns	15pF, 50pF	t_{PLH}, t_{PHL}



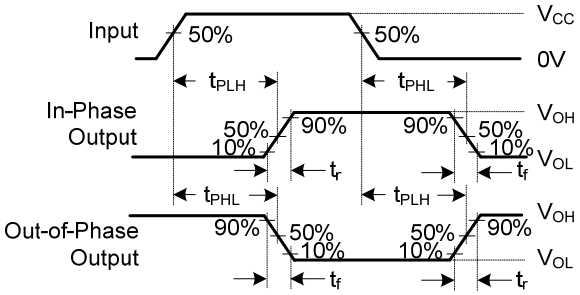
Voltage Waveforms Setup And
Hold And Input Rise And Fall Times



Voltage Waveforms Pulse Durations



Test Circuit for Measuring Switching Times



Voltage Waveforms
Propagation Delay And Output Transition Times

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤1MHz, Z_O = 50Ω.