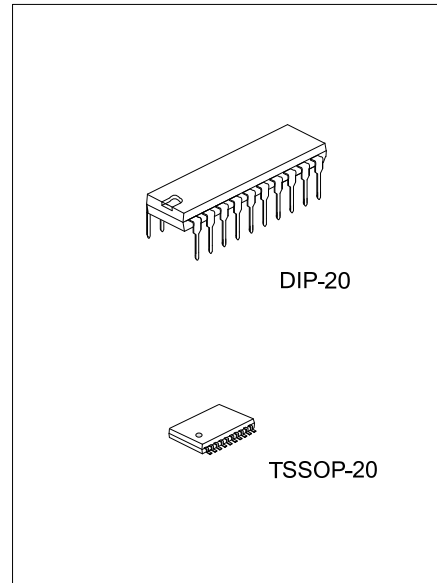




U74HCT541

CMOS IC

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS



DESCRIPTION

The **U74HCT541** is octal buffers and line drivers are with 3-state outputs and 8 channels.

The 3-state control gate is a 2-input NOR. If either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state. The **U74HCT541** devices provide true data at the outputs.

FEATURES

- * Operating Voltage Range of 4.5V to 5.5V
- * High-Current 3-State Outputs Interface Directly With System Bus or Can Drive Up To 15 LSTTL Loads
- * Low Power Consumption I_{CC} : 4 μ A (Max.)
- * Typical t_{pd} =13ns
- * ± 6 mA Output Drive at 5V
- * Low Input Current of 1uA max
- * Inputs Are TTL-Voltage Compatible
- * Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)

ORDERING INFORMATION

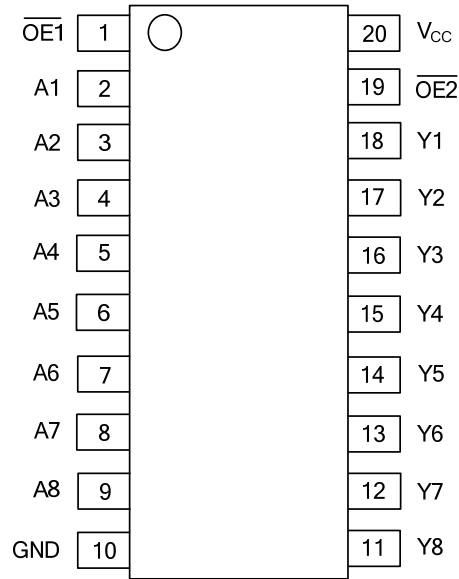
| Ordering Number | | Package | Packing |
|------------------|------------------|----------|-----------|
| Lead Free | Halogen Free | | |
| U74HCT541L-D20-T | U74HCT541G-D20-T | DIP-20 | Tube |
| - | U74HCT541G-P20-R | TSSOP-20 | Tape Reel |

| | |
|--|---|
| <p>U74HCT541L-D20-T</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p> | <p>(1) T: Tube, R: Tape Reel (2) D20: DIP-20, P20: TSSOP-20 (3) L: Lead Free, G: Halogen Free and Lead Free</p> |
|--|---|

MARKING

| DIP-20 | TSSOP-20 |
|---|---|
| <p>UTC □□□□ U74HCT541 □ □□</p> <p>→ Date Code → L: Lead Free → G: Halogen Free → Lot Code</p> | <p>UTC □□□□ U74HCT541G □□</p> <p>→ Date Code → Lot Code</p> |

■ PIN CONFIGURATION

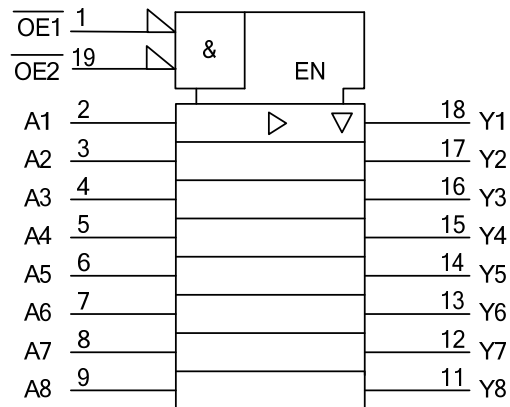


■ FUNCTION TABLE

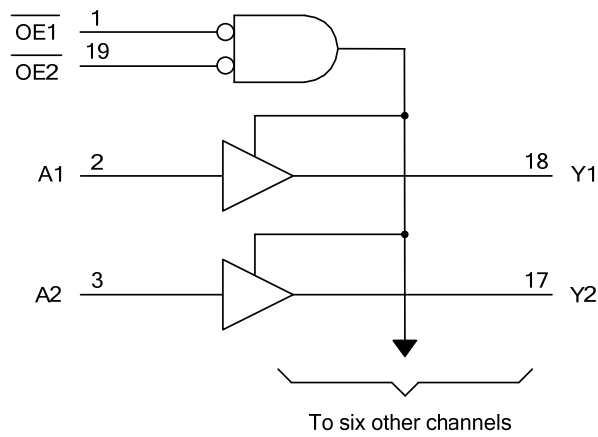
| INPUTS($\overline{OE1}$) | INPUTS($\overline{OE2}$) | INPUTS(A) | OUTPUT(Y) |
|----------------------------|----------------------------|-----------|-----------|
| L | L | L | L |
| L | L | H | H |
| H | X | X | Z |
| X | H | X | Z |

Note: H: HIGH Voltage Level L: LOW Voltage Level Z: High Impedance X: Don' Care

■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING

| PARAMETER | SYMBOL | RATINGS | UNIT |
|-------------------------|-----------|-------------|------|
| Supply Voltage | V_{CC} | -0.5 ~ 7 | V |
| Input Voltage | V_{IN} | -0.5 ~ 7 | V |
| V_{CC} or GND Current | I_{CC} | ±70 | mA |
| Output Current | I_{OUT} | ±35 | mA |
| Input Clamp Current | I_{IK} | ±20 | mA |
| Output Clamp Current | I_{OK} | ±20 | mA |
| Operating Temperature | T_A | -40 ~ + 85 | °C |
| Storage Temperature | T_{STG} | -65 ~ + 150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---------------------|----------|---------|------|
| Junction to Ambient | DIP-20 | 69 | °C/W |
| | TSSOP-20 | 83 | °C/W |

■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|---------------------|------------------------|-----|-----|----------|------|
| Supply Voltage | V_{CC} | | 4.5 | 5 | 5.5 | V |
| High-level Input Voltage | V_{IH} | $V_{CC}=4.5V\sim 5.5V$ | 2 | | | V |
| Low-level Input Voltage | V_{IL} | $V_{CC}=4.5V\sim 5.5V$ | | | 0.8 | V |
| Input Voltage | V_{IN} | | 0 | | V_{CC} | V |
| Output Voltage | V_{OUT} | | 0 | | V_{CC} | V |
| Input transition Rise or Fall rate | $\Delta t/\Delta v$ | | | | 500 | ns |

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ C$)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|--|------|-------|------|------|
| High-Level Output Voltage | V_{OH} | $V_{CC}=4.5V, V_I=V_{IH}$ or $V_{IL}, I_{OH}=-20\mu A$ | 4.4 | 4.499 | | V |
| | | $V_{CC}=5.5V, V_I=V_{IH}$ or $V_{IL}, I_{OH}=-20\mu A$ | 5.4 | 5.499 | | |
| | | $V_{CC}=4.5V, V_I=V_{IH}$ or $V_{IL}, I_{OH}=-6mA$ | 3.98 | 4.3 | | |
| Output Voltage Low-Level | V_{OL} | $V_{CC}=4.5V, V_I=V_{IH}$ or $V_{IL}, I_{OL}=20\mu A$ | | 0.001 | 0.1 | V |
| | | $V_{CC}=5.5V, V_I=V_{IH}$ or $V_{IL}, I_{OL}=20\mu A$ | | 0.001 | 0.1 | |
| | | $V_{CC}=4.5V, V_I=V_{IH}$ or $V_{IL}, I_{OL}=6mA$ | | 0.17 | 0.26 | |
| Input Leakage Current | $I_{I(LEAK)}$ | $V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND | | ±0.1 | ±100 | nA |
| 3-state Output Off-state Current | I_{OZ} | $V_{CC}=5.5V, V_{OUT}=V_{CC}$ or GND, $V_I=V_{IH}$ or V_{IL} | | ±0.01 | ±0.5 | μA |
| Quiescent Supply Current | I_{CC} | $V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$ | | | 4 | μA |
| Additional Quiescent Device Current Per Input Pin | ΔI_{CC} | $V_{CC}=5.5V$, One input at 0.5V or 2.4V Other inputs at 0 or V_{CC} | | 1.4 | 2.4 | mA |
| Input Capacitance | C_I | $V_{CC}=4.5V\sim 5.5V$ | | 3 | 10 | pF |

■ SWITCHING CHARACTERISTICS ($T_A=25^\circ C, C_L=50pF$)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|-------------------|-----------------|-----|-----|-----|------|
| From A to Y | t_{PLH}/t_{PHL} | $V_{CC}=4.5V$ | | 13 | 23 | ns |
| | | $V_{CC}=5.5V$ | | 13 | 21 | |
| From \overline{OE} to Y | t_{PZL}/t_{PZH} | $V_{CC}=4.5V$ | | 21 | 30 | ns |
| | | $V_{CC}=5.5V$ | | 19 | 27 | |
| From \overline{OE} to Y | t_{PLZ}/t_{PHZ} | $V_{CC}=4.5V$ | | 19 | 30 | ns |
| | | $V_{CC}=5.5V$ | | 18 | 27 | |

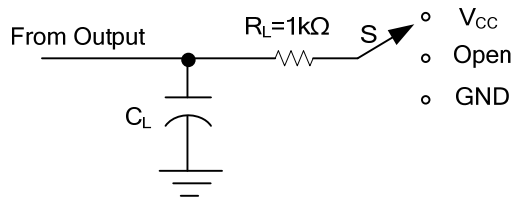
■ SWITCHING CHARACTERISTICS (T_A=25°C, C_L=150pF)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|------------------------------------|-----------------------|-----|-----|-----|------|
| Y | t _t | V _{CC} =4.5V | | 8 | 12 | ns |
| | | V _{CC} =5.5V | | 7 | 11 | |
| From A to Y | t _{PLH} /t _{PHL} | V _{CC} =4.5V | | 20 | 33 | ns |
| | | V _{CC} =5.5V | | 19 | 30 | |
| From \overline{OE} to Y | t _{PZL} /t _{PZH} | V _{CC} =4.5V | | 26 | 40 | ns |
| | | V _{CC} =5.5V | | 25 | 36 | |
| Y | t _t | V _{CC} =4.5V | | 17 | 42 | ns |
| | | V _{CC} =5.5V | | 14 | 38 | |

■ OPERATING CHARACTERISTICS (T_A=25°C)

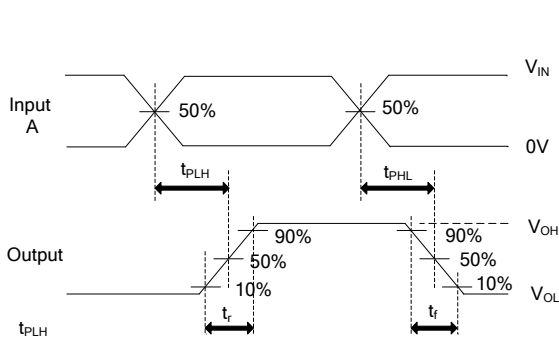
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|-----------------|-----|-----|-----|------|
| Power Dissipation Capacitance Per buffer/driver | C _{PD} | No Load | | 35 | | pF |

■ TEST CIRCUIT AND WAVEFORMS

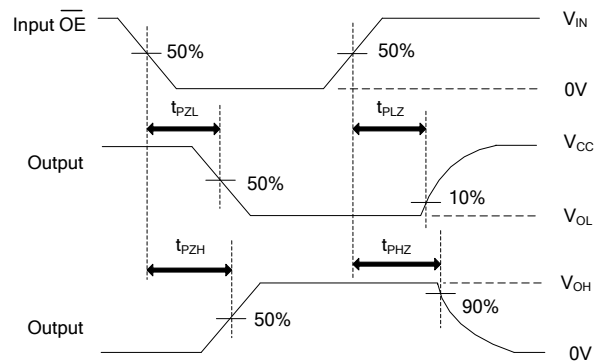


| TEST | S |
|-------------------|----------|
| t_{PLH}/t_{PHL} | Open |
| t_{PHZ}/t_{PZH} | GND |
| t_{PLZ}/t_{PZL} | V_{CC} |

TEST CIRCUIT



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

- Notes: 1. C_L includes probe and test-fixture capacitance.
 2. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{MHz}$, $Z_o=50\Omega$, $t_r=6\text{ns}$, $t_f=6\text{ns}$.

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