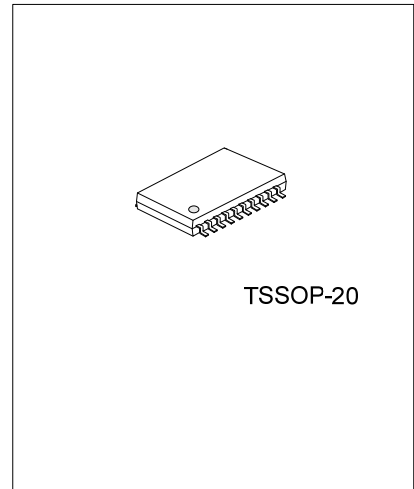




## U74HCT574

CMOS IC

### OCTAL D-TYPE EDGE-TRIGGER FLIP-FLOP WITH 3-STATE OUTPUT



#### DESCRIPTION

The UTC **74HCT574** is octal D-type flip-flop featuring separate D-type inputs for each flip-flop and non-inverting 3-state outputs for bus-oriented applications.

#### FEATURES

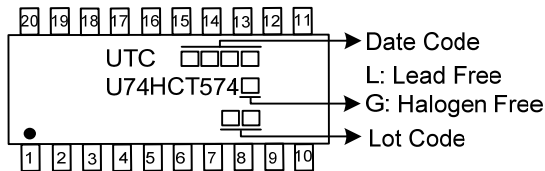
- \* Operation Voltage Range:4.5V~5.5V
- \* 3-state Non-Inverting Outputs for Bus-oriented Applications
- \* Common 3-state Output Enable Input
- \* Inputs are TTL voltage compatible

#### ORDERING INFORMATION

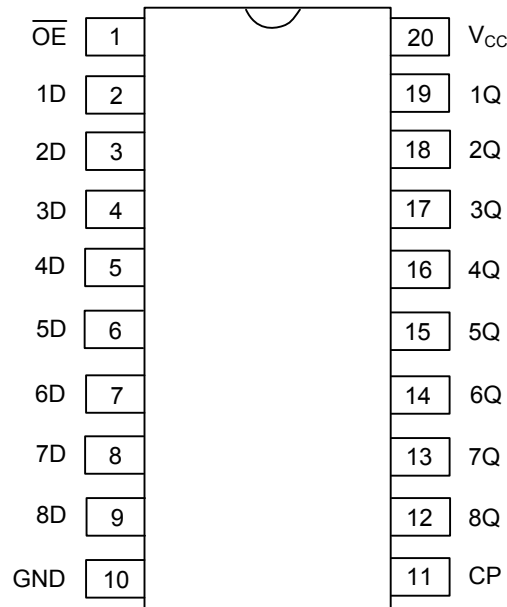
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT574L-P20-R	U74HCT574G-P20-R	TSSOP-20	Tape Reel

<p>U74HCT574G-P20-R</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) R: Tape Reel (2) P20: TSSOP-20 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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#### MARKING



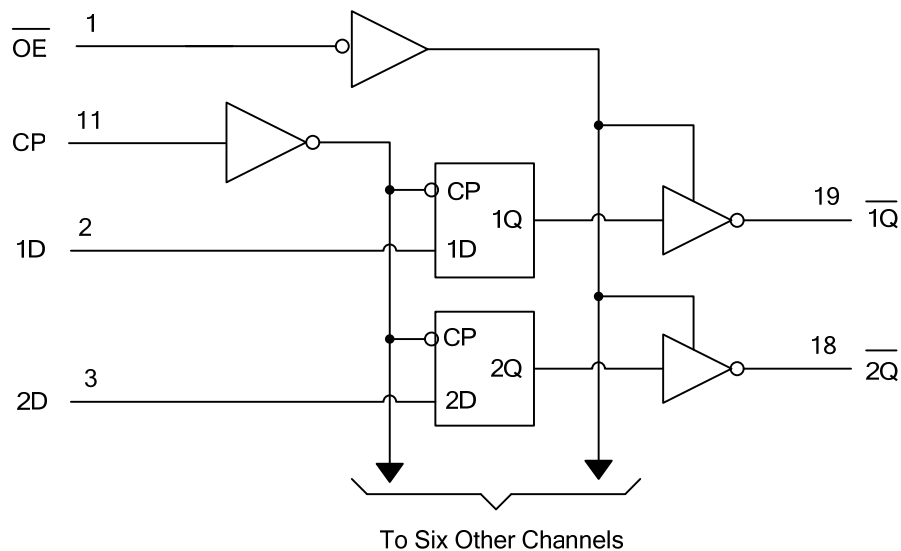
■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUTS( $\overline{OE}$ )	INPUTS(CP)	INPUTS(D)	OUTPUT(Q)
L	↑	H	H
L	↑	L	L
L	L or H	X	Q0
H	X	X	Z

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING(unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	-0.5~7.0	V
Input Voltage	$V_{IN}$	-0.5~ $V_{CC}+0.5$	V
Output Voltage(active mode)	$V_{OUT}$	-0.5~ $V_{CC}+0.5$	V
Input Clamp Current ( $V_{IN}<0$ )	$I_{IK}$	±20	mA
Output Clamp Current ( $V_{OUT}<0$ )	$I_{OK}$	±20	mA
Output Current	$I_{OUT}$	±35	mA
$V_{CC}$ or GND Current	$I_{CC}$	±50	mA
Storage Temperature	$T_{STG}$	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	4.5 ~ 5.5	V
Input Voltage	$V_{IN}$	0 ~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0 ~ $V_{CC}$	V
Operating Temperature	$T_{OPR}$	-40 ~ 85	°C
Input Transition Rise or Fall Rate	$t_T$	0 ~ 500	ns

■ ELECTRICAL CHARACTERISTICS( $T_A=25^{\circ}C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level input voltage	$V_{IH}$	$V_{CC}=4.5V\sim 5.5V$	2.0	1.6		V
Low-Lever output voltage	$V_{IL}$	$V_{CC}=4.5V\sim 5.5V$		1.2	0.8	V
High-Level Output Voltage	$V_{OH}$	$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4	4.499		V
		$V_{CC}=4.5V, I_{OH}=-6mA$	3.98	4.3		V
Low-Level Output Voltage	$V_{OL}$	$V_{CC}=4.5V, I_{OL}=20\mu A$		0.001	0.1	V
		$V_{CC}=4.5V, I_{OL}=6mA$		0.17	0.26	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND		±0.1	±100	nA
Output OFF -state current	$I_{OZ}$	$V_{CC}=5.5V, V_{OUT}=V_{CC}$ or GND		±0.01	±0.5	μA
Quiescent Supply Current	$I_{CC}$	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			8	μA
Additional Quiescent Supply Current	$\Delta I_{CC}$	$V_{CC}=5.5V$ , One input at 0.5V or 2.4V, other inputs at 0 or $V_{CC}$		100	360	μA
Input Capacitance	$C_{IN}$	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND		3	10	pF

■ TIMING REQUIREMENTS ( $T_A=25^\circ\text{C}$ ,  $C_L=50\text{pF}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pulse duration, LE high	$t_W$	$V_{CC}=4.5V$	16	7		ns
Setup Time, data before LE ↓	$t_{SU}$	$V_{CC}=4.5V$	12	3		ns
Hold Time, data after LE ↓	$t_H$	$V_{CC}=4.5V$	5	-1		ns

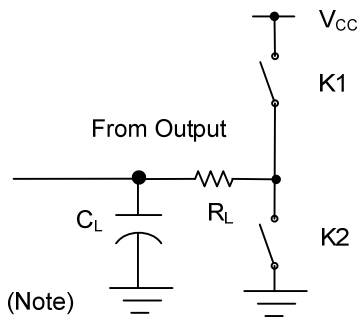
■ DYNAMIC CHARACTERISTICS ( $T_A=25^\circ\text{C}$ ,  $C_L=50\text{pF}$ ,  $R_L=1\text{k}\Omega$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (CP) to output ( $\bar{Q}$ )	$t_{PD}$ ( $t_{PLH}/t_{PHL}$ )	$V_{CC}=4.5V$		18	33	ns
3-state output enable time from input ( $\overline{OE}$ ) to output ( $\bar{Q}$ )	$t_{EN}$ ( $t_{PZL}/t_{PZH}$ )	$V_{CC}=4.5V$		19	33	ns
3-state output disable time from input ( $\overline{OE}$ ) to output ( $\bar{Q}$ )	$t_{DIS}$ ( $t_{PLZ}/t_{PHZ}$ )	$V_{CC}=4.5V$		16	28	ns
Output transition time, ( $\bar{Q}$ )	$t_T$ ( $t_R/t_F$ )	$V_{CC}=4.5V$		5	12	ns

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power Dissipation Capacitance	$C_{PD}$	No load	50	pF

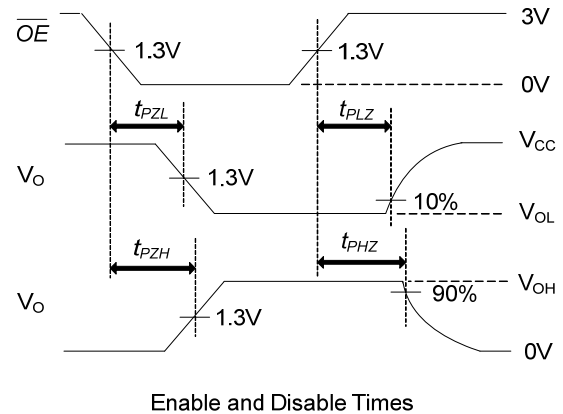
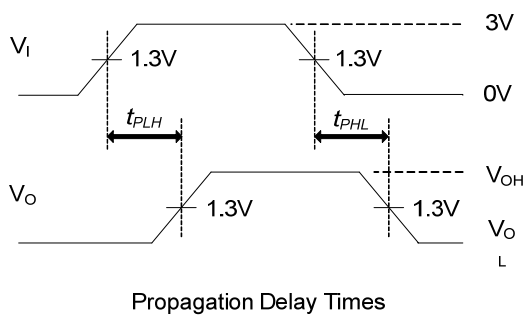
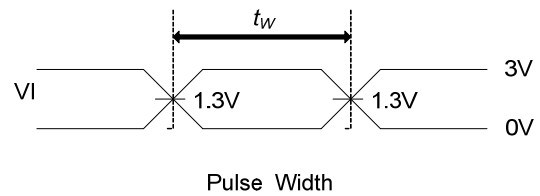
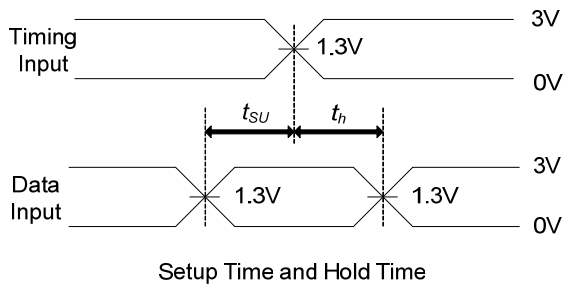
## TEST CIRCUIT AND WAVEFORMS



TEST	K1	K2
$t_{PLH}/t_{PHL}$	Open	Open
$t_{PHZ}/t_{PZH}$	Open	Close
$t_{PLZ}/t_{PZL}$	Close	Open

Note:  $C_L$  includes probe and jig capacitance.

$$P_{RR} \leq 1\text{MHz}, Z_0 = 50\Omega, t_r \leq 6\text{ns}, t_f \leq 6\text{ns}$$



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