



U74LVC00A

CMOS IC

QUAD 2-INPUT NAND GATE

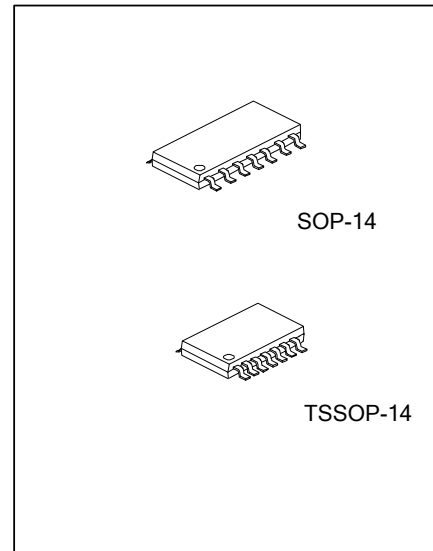
DESCRIPTION

The **U74LVC00A** is a quad 2-input NAND gate which performs the Function $Y=A \bullet B$ or $Y=\overline{A + B}$ in positive logic circuit.

This device has power-down protective circuit to prevent the device from destruction when it is powered down.

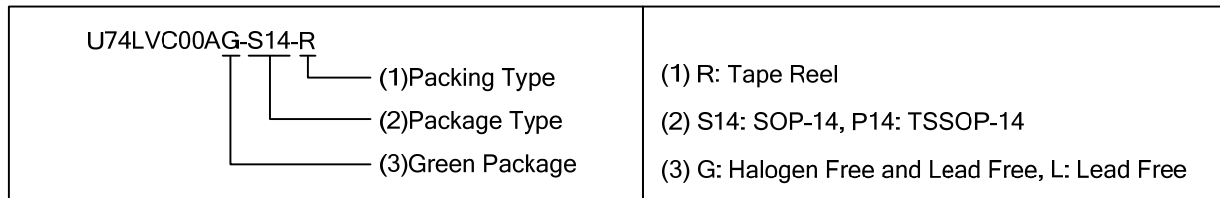
FEATURES

- * Operate From 1.5V to 3.6V
- * Inputs Accept Voltages to 5.5V
- * High Noise Immunity
- * Low Power Dissipation
- * Max t_{PD} of 5 ns at 3.3V

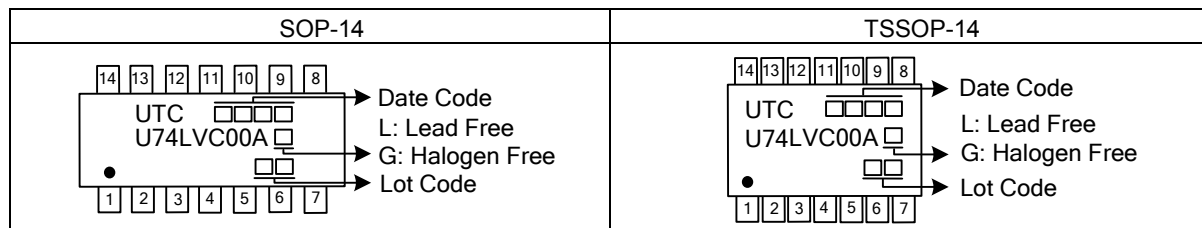


ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC00AL-S14-R	U74LVC00AG-S14-R	SOP-14	Tape Reel
U74LVC00AL-P14-R	U74LVC00AG-P14-R	TSSOP-14	Tape Reel



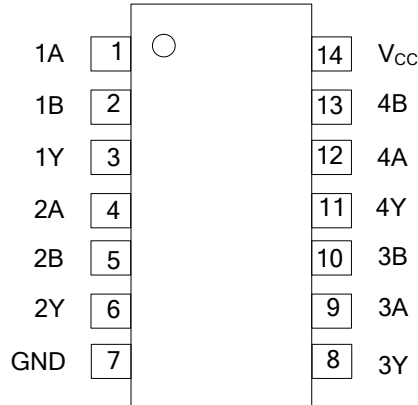
MARKING



U74LVC00A

CMOS IC

■ PIN CONFIGURATION

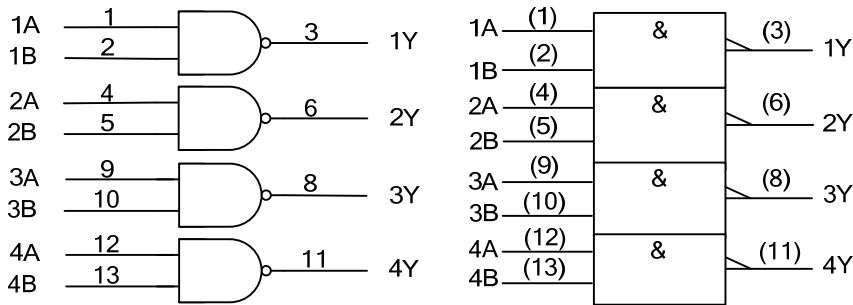


■ FUNCTION TABLE

INPUT(nA)	INPUT(nB)	OUTPUT(nY)
H	H	L
H	L	H
L	H	H
L	L	H

Note: H: HIGH voltage level; L: LOW voltage level.

■ LOGIC DIAGRAM (Positive Logic)



Logic Symbol

IEC Logic Symbol



U74LVC00A

CMOS IC

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 6.5	V
Input Voltage	V_{IN}	-0.5 ~ 6.5	V
Output Voltage	V_{OUT}	-0.5 ~ $V_{CC}+0.5$	V
V_{CC} or GND Current (Output In The Power-Off State)	I_{CC}	±100	mA
Continuous Output Current ($V_{OUT}=0$ to V_{CC})	I_{OUT}	±50	mA
Input Clamp Current ($V_{IN}<0$)	I_{IK}	-50	mA
Output Clamp Current ($V_{OUT}<0$ or $V_{OUT}>V_{CC}$)	I_{OK}	-50	mA
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		3.6	V
High-Level Input Voltage	V_{IH}	$V_{CC}=1.65V$ to $1.95V$	$0.65 \cdot V_{CC}$			V
		$V_{CC}=2.3V$ to $2.7V$	1.7			
		$V_{CC}=2.7V$ to $3.6V$	2			
Low-Level Input Voltage	V_{IL}	$V_{CC}=1.65V$ to $1.95V$			$0.35 \cdot V_{CC}$	V
		$V_{CC}=2.3V$ to $2.7V$			0.7	
		$V_{CC}=2.7V$ to $3.6V$			0.8	
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Ambient Temperature	T_A		-40		85	°C

■ ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
High-Level Output Voltage	V_{OH}	$I_{OH}=-100\mu A$, $V_{CC}=1.65V$ to $3.6V$	$V_{CC}-0.2$			V	
		$I_{OH}=-4mA$, $V_{CC}=1.65V$	1.2			V	
		$I_{OH}=-8mA$, $V_{CC}=2.3V$	1.7			V	
		$I_{OH}=-12mA$	$V_{CC}=2.7V$	2.2			V
			$V_{CC}=3V$	2.4			
Low-Level Output Voltage	V_{OL}	$I_{OL}=100\mu A$, $V_{CC}=1.65V$ to $3.6V$			0.2	V	
		$I_{OH}=4mA$, $V_{CC}=1.65V$			0.45		
		$I_{OH}=8mA$, $V_{CC}=2.3V$			0.7		
		$I_{OL}=12mA$, $V_{CC}=2.7V$			0.4	V	
		$I_{OL}=24mA$, $V_{CC}=3.0V$			0.55	V	
Input Leakage Current	$I_{I(LEAK)}$	$V_{IN}=5.5V$ or GND, $V_{CC}=3.6V$			±5	μA	
Quiescent Supply Current	I_Q	$V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$, $V_{CC}=3.6V$			10	μA	
Additional Quiescent Supply Current Per Input Pin	ΔI_Q	$V_{CC}=2.7 \sim 3.6V$, One input at $V_{CC}-0.6V$, Other inputs at V_{CC} or GND, $I_{OUT}=0$			500	μA	
Input Capacitance	C_{IN}	$V_{IN}=V_{CC}$ or GND		5		pF	



U74LVC00A

CMOS IC

■ SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From Input (nA or nB) To Output(nY)	t_{PD}	$V_{CC}=2.7\text{V}$, $R_L=500\Omega$	1		5.1	ns
		$V_{CC}=3.3\pm 0.3\text{V}$, $R_L=500\Omega$			$C_L=50\text{pF}$	4.3

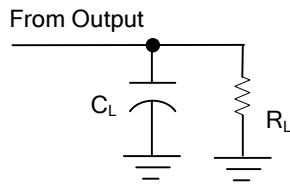
■ OPERATING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	UNIT
Power Dissipation Capacitance	C_{PD}	$V_{CC}=3.3\text{V}\pm 0.3\text{V}$, $C_L=50\text{pF}$, $f=10\text{MHz}$	9.5	pF

U74LVC00A

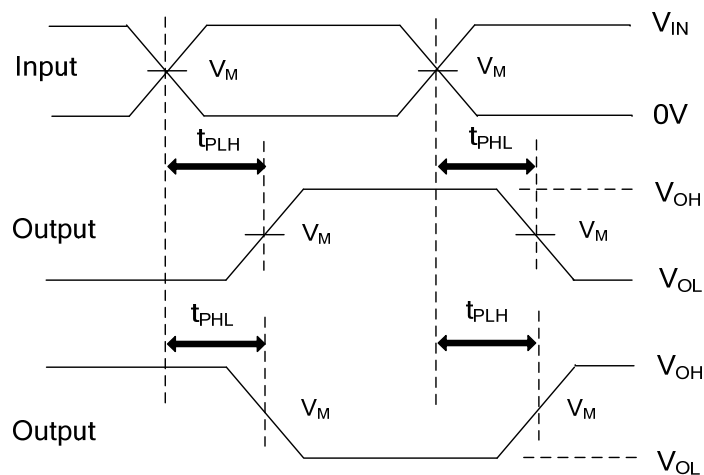
CMOS IC

TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

V_{CC}	INPUTS		V_M	C_L	R_L
	V_{IN}	t_R / t_F			
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	30pF	1K Ω
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	30pF	500 Ω
2.7V	2.7V	$\leq 2.5ns$	1.5V	50pF	500 Ω
$3.3V \pm 0.3V$	2.7V	$\leq 2.5ns$	1.5V	50pF	500 Ω



PROPAGATION DELAY TIMES

Note: C_L includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR $\leq 10MHz$, $Z_o = 50\Omega$.

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.