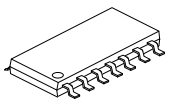
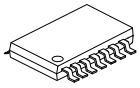
# U74LVC09A

**CMOS IC**

## QUAD 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT



SOP-14



TSSOP-14

## ■ DESCRIPTION

The **U74LVC09A** provides four 2-input NAND functions.The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs can be driven from either 3.3V or 5.5V devices.This feature allows the use of these devices as translators in mixed 3.3V and 5V applications.

## ■ FEATURES

* Operate From 1.65V to 5.5V
* Input Accept Voltages to 5.0V
* Partial-Power-Down Mode Operation
* Max tpd is 3.6ns at 3.3V

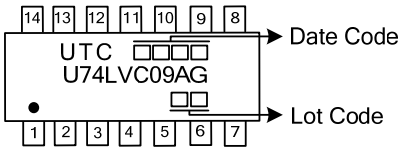
## ■ ORDERING INFORMATION

| Ordering Number | Package | Packing |
|---|---|---|
| U74LVC09AG-S16-R | SOP-16 | Tape Reel |

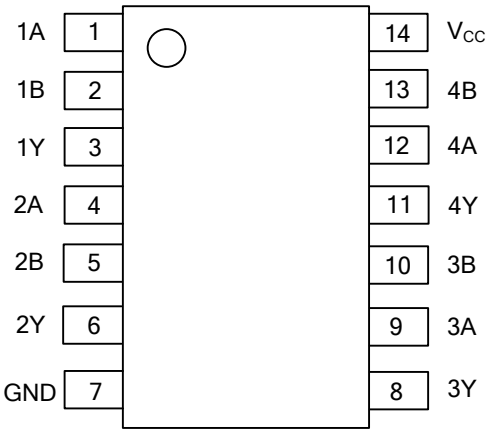
U74LVC09AG-S16-R
- (1)Packing Type
- (2)Package Type
- (3)Green Package

(1) R: Tape Reel
(2) S16: SOP-16
(3) G: Halogen Free and Lead Free

## ■ MARKING



## ■ PIN CONFIGURATION

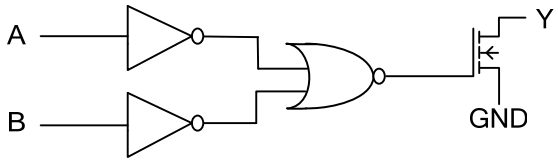



## ■ FUNCTION TABLE **(each gate)**

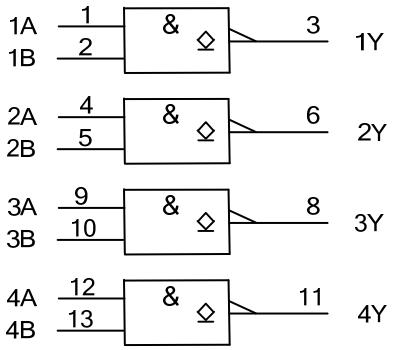
| INPUT(nA) | INPUT(nB) | OUTPUT(nY) |
|---|---|---|
| L | L | Z |
| L | H | Z |
| H | L | Z |
| H | H | L |

H = High voltage level
L = Low voltage level
Z = High-impedance OFF-state

## ■ LOGIC DIAGRAM (Positive Logic)




Logic symbol




IEC logic symbol

## ■ ABSOLUTE MAXIMUM RATING

| PARAMETER | SYMBOL | CONDITIONS | RATINGS | UNIT |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | -0.5 ~ +6.5 | V |
| Input Voltage | $V_{IN}$ | | -0.5 ~ +6.5 | V |
| Output Voltage | $V_{OUT}$ | Output in the high or low state | -0.5 ~ $V_{CC}$ +0.5 | V |
| | | Output in the power-off state | -0.5 ~ +6.5 | V |
| Continuous $V_{CC}$ or GND Current | $I_{CC}$ | | -50 | mA |
| Continuous Output Current | $I_{OUT}$ | $V_{OUT}$=0V ~ $V_{CC}$ | ±50 | mA |
| Input Clamp Current | $I_{IK}$ | $V_{IN}$<0V | 50 | mA |
| Output Clamp Current | $I_{OK}$ | $V_{OUT}$>$V_{CC}$ or $V_{OUT}$<0V | ±100 | mA |
| Storage Temperature Range | $T_{STG}$ | | -65 ~ +150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | Operating | 1.65 | | 5.5 | V |
| | | Data retention only | 1.2 | | | V |
| Input Voltage | $V_{IN}$ | | 0 | | 5.5 | V |
| Output Voltage | $V_{OUT}$ | High or low state | 0 | | $V_{CC}$ | V |
| | | 3-state | 0 | | 5.5 | V |
| Operating Temperature (Note) | $T_A$ | | -40 | | 125 | °C |
| Input Transition Rise or Fall Rate | Δt/Δv | $V_{CC}$=1.65V ~ 2.7V | 0 | | 20 | ns/V |
| | | $V_{CC}$=2.7V ~ 3.6V | 0 | | 10 | ns/V |

Note: This condition is only determined from design. It can't be 100% tested in mass production.

## ■ ELECTRICAL CHARACTERISTICS ($T_A$ =25°C , unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| High-level Input Voltage | $V_{IH}$ | $V_{CC}$=1.8V±0.15V | 0.65×$V_{CC}$ | | | V |
| | | $V_{CC}$=2.5V±0.2V | 1.7 | | | V |
| | | $V_{CC}$=3.3V±0.3V | 2 | | | V |
| | | $V_{CC}$=5.0V±0.5V | 0.7×$V_{CC}$ | | | V |
| Low-level Input Voltage | $V_{IL}$ | $V_{CC}$=1.8V±0.15V | | | 0.35×$V_{CC}$ | V |
| | | $V_{CC}$=2.5V±0.2V | | | 0.7 | V |
| | | $V_{CC}$=3.3V±0.3V | | | 0.8 | V |
| | | $V_{CC}$=5.0V±0.5V | | | 0.3×$V_{CC}$ | V |
| Low-Level Output Voltage | $V_{OL}$ | $V_{CC}$=1.65V ~ 5.5V, $I_{OH}$=100μA | | | 0.2 | V |
| | | $V_{CC}$=1.65V, $I_{OH}$=4mA | | | 0.45 | V |
| | | $V_{CC}$=2.3V, $I_{OH}$=8mA | | | 0.6 | V |
| | | $V_{CC}$=2.7V, $I_{OH}$=12mA | | | 0.4 | V |
| | | $V_{CC}$=3.0V, $I_{OH}$=24mA | | | 0.55 | V |
| | | $V_{CC}$=4.5V, $I_{OH}$=32mA | | | 0.55 | V |
| Input Leakage Current | $I_{I(LEAK)}$ | $V_{CC}$=1.65V ~ 5.5V, $V_{IN}$=5.5V or GND | | ±0.1 | ±5 | μA |
| Power OFF Leakage Current | $I_{off}$ | $V_{CC}$=0V, $V_{IN}$ or $V_{OUT}$=5.5V | | ±0.1 | ±10 | uA |
| Input Leakage Current (For I/O Ports) | $I_{OZ}$ | $V_{CC}$=1.65V ~ 5.5V, $V_{IN}$ = $V_{IH}$, $V_{OUT}$=GND to 5.5V | | 0.1 | ±5 | μA |
| Quiescent Supply Current | $I_{CC}$ | $V_{CC}$=5.5V, $V_{IN}$=5.5V or GND, $I_{OUT}$=0A | | 0.1 | 10 | μA |
| Additional Quiescent Supply Current Per Input Pin | $\Delta I_{CC}$ | $V_{CC}$=2.7V~5.5V, Per input pin, $V_I$=$V_{CC}$-0.6V, $I_O$=0A | | 5 | 500 | μA |
| Input Capacitance | $C_I$ | $V_{CC}$=0V to 5.5V, $V_{IN}$=$V_{CC}$ or GND | | 4.0 | | pF |

## ■ SWITCHING CHARACTERISTICS ($T_A$ =25°C , unless otherwise specified)

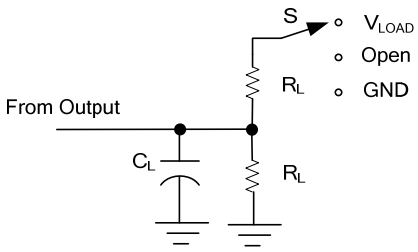
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Propagation delay from input (nA or nB) to output(Y) | $t_{PZL}$ | $V_{CC}$=1.8V±0.15V, $C_L$=30pF, $R_L$=1KΩ | 1.0 | 2.6 | 6.0 | ns |
| | | $V_{CC}$=2.5V±0.2V, $C_L$=30pF, $R_L$=500Ω | 0.5 | 1.8 | 3.3 | ns |
| | | $V_{CC}$=2.7V, $C_L$=50pF, $R_L$=500Ω | 0.5 | 1.7 | 2.9 | ns |
| | | $V_{CC}$=3.3V±0.3V, $C_L$=50pF, $R_L$=500Ω | 0.5 | 1.8 | 3.0 | ns |
| Propagation delay from input (nA or nB) to output(Y) | $t_{PLZ}$ | $V_{CC}$=1.8V±0.15V, $C_L$=30pF, $R_L$=1KΩ | 1.0 | 2.7 | 6.0 | ns |
| | | $V_{CC}$=2.5V±0.2V, $C_L$=30pF, $R_L$=500Ω | 0.5 | 1.5 | 3.3 | ns |
| | | $V_{CC}$=2.7V, $C_L$=50pF, $R_L$=500Ω | 1.0 | 2.6 | 3.8 | ns |
| | | $V_{CC}$=3.3V±0.3V, $C_L$=50pF, $R_L$=500Ω | 1.0 | 2.3 | 3.6 | ns |
| Output skew time | $t_{sw}$ | | | | 1.0 | ns |

## ■ OPERATING CHARACTERISTICS

(Per gate, $V_{IN}$=GND or $V_{CC}$, f=10MHz , $T_A$ =25°C, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Power Dissipation Capacitance | $C_{PD}$ | $V_{CC}$=1.8V±0.15V, $C_L$=30pF | | 6.2 | | pF |
| | | $V_{CC}$=2.5V±0.2V, $C_L$=30pF | | 9.7 | | pF |
| | | $V_{CC}$=3.3V±0.3V, $C_L$=50pF | | 12.9 | | pF |

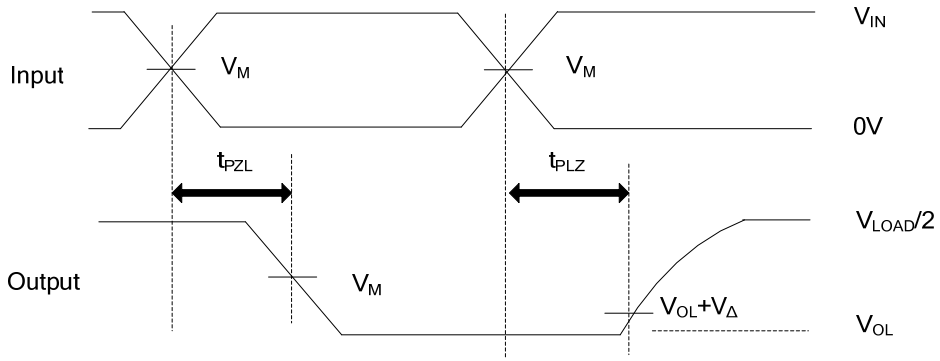
## ■ TEST CIRCUIT AND WAVEFORMS




TEST CIRCUIT

| TEST | S |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PHZ}/t_{PZH}$ | GND |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |

| $V_{CC}$ | INPUTS | | $V_M$ | $V\triangle$ | $C_L$ | $R_L$ |
|---|---|---|---|---|---|---|
| | $V_{IN}$ | $t_R/t_F$ | | | | |
| 1.8V±0.15V | $V_{CC}$ | ≤2ns | Vcc/2 | 0.15V | 30pF | 1KΩ |
| 2.5V±0.2V | $V_{CC}$ | ≤2ns | Vcc/2 | 0.15V | 30pF | 500Ω |
| 2.7V | 2.7V | ≤2.5ns | 1.5V | 0.3V | 50pF | 500Ω |
| 3.3V±0.3V | 2.7V | ≤2.5ns | 1.5V | 0.3V | 50pF | 500Ω |




ENABLE AND DISABLE TIMES

Notes: 1. $C_L$ includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, $Z_O$ = 50Ω.