



U74LVC1G79

CMOS IC

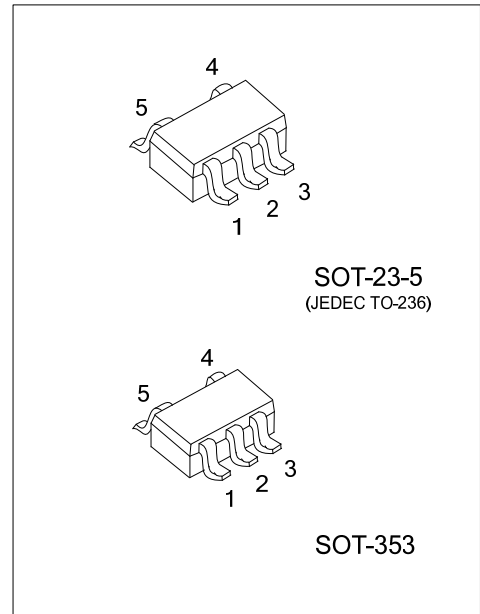
SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

■ DESCRIPTION

The **U74LVC1G79** is a single positive-edge-triggered D-type flip-flop.

When data at the data input (D) meets the set-up time requirements, the data is transferred to the outputs (Q) on the positive-going edge of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the level at the outputs.

This device has power-down protective circuit, preventing device destruction when it is powered down.



■ FEATURES

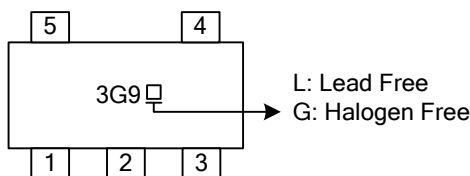
- * Operate from 1.65V to 5.5V
- * Inputs accept voltages to 5.5V
- * I_{off} supports partial-power-down mode
- * Low power dissipation: I_{CC}=10μA (Max.)
- * ±24mA output drive(V_{CC}=3.3V)

■ ORDERING INFORMATION

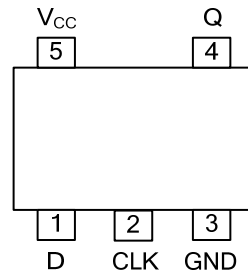
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC1G79G-AE5-R	U74LVC1G79G-AE5-R	SOT-23-5	Tape Reel
U74LVC1G79G-AL5-R	U74LVC1G79G-AL5-R	SOT-353	Tape Reel

<p>U74LVC1G79G-AE5-R</p>	<p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) AE5: SOT-23-5, AL5: SOT-353</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



■ PIN CONFIGURATION

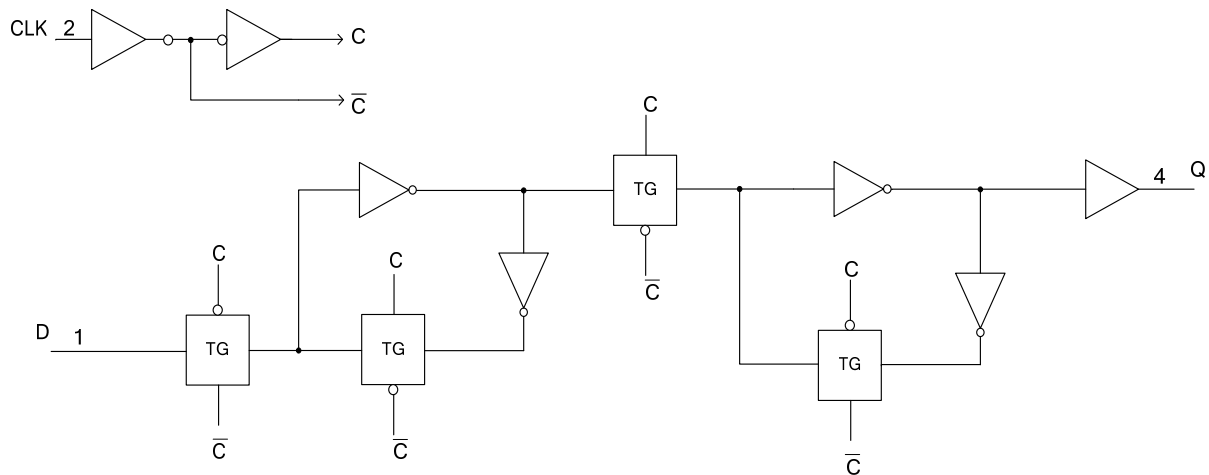


■ FUNCTION TABLE (EACH GATE)

INPUT		OUTPUT
CLK	D	Q
↑	H	H
↑	L	L
L	X	Q ₀

Note: H: HIGH voltage level; L: LOW voltage level; X: Don't care; ↑: Low to High CLK transition
 Q₀: indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CLK transition

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5 ~ +6.5	V
Input Voltage		V_{IN}	-0.5 ~ +6.5	V
Output Voltage	Output in the high or low state	V_{OUT}	-0.5 ~ $V_{CC}+0.5$	V
	Output in the high-impedance or power-off state		-0.5 ~ +6.5	V
V_{CC} or GND Current		I_{CC}	±100	mA
Continuous Output Current ($V_{OUT}=0 \sim V_{CC}$)		I_{OUT}	±50	mA
Input Clamp Current ($V_{IN}<0$)		I_{IK}	-50	mA
Output Clamp Current ($V_{OUT}<0$)		I_{OK}	-50	mA
Storage Temperature Range		T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
High-Level Input Voltage	V_{IH}	$V_{CC}=1.65V\sim 1.95V$	$0.65 \times V_{CC}$			V
		$V_{CC}=2.3V\sim 2.7V$	1.7			
		$V_{CC}=3.0V\sim 3.6V$	2			
		$V_{CC}=4.5V\sim 5.5V$	$0.7 \times V_{CC}$			
Low-Level Input Voltage	V_{IL}	$V_{CC}=1.65V\sim 1.95V$			$0.35 \times V_{CC}$	V
		$V_{CC}=2.3V\sim 2.7V$			0.7	
		$V_{CC}=3.0V\sim 3.6V$			0.8	
		$V_{CC}=4.5V\sim 5.5V$			$0.3 \times V_{CC}$	
High-level Output Current	I_{OH}	$V_{CC}=1.65V$			-4	mA
		$V_{CC}=2.3V$			-8	mA
		$V_{CC}=3.0V$			-16	mA
		$V_{CC}=3.0V$			-24	mA
		$V_{CC}=4.5V$			-32	mA
Low-level Output Current	I_{OL}	$V_{CC}=1.65V$			4	mA
		$V_{CC}=2.3V$			8	mA
		$V_{CC}=3.0V$			16	mA
		$V_{CC}=3.0V$			24	mA
		$V_{CC}=4.5V$			32	mA
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=1.65V\sim 1.95V, 2.3V\sim 2.7V$			20	ns/V
		$V_{CC}=3.0V\sim 3.6V$			10	ns/V
		$V_{CC}=4.5V\sim 5.5V$			5	ns/V
Operating Temperature	T_A		-40		85	°C

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V _{OH}	V _{CC} =1.65V~5.5V, I _{OH} =-100μA	V _{CC} -0.1			V
		V _{CC} =1.65V, I _{OH} =-4mA	1.2			
		V _{CC} =2.3V, I _{OH} =-8mA	1.9			
		V _{CC} =3.0V, I _{OH} =-16mA	2.4			
		V _{CC} =3.0V, I _{OH} =-24mA	2.3			
		V _{CC} =4.5V, I _{OH} =-32mA	3.8			
Low-Level Output Voltage	V _{OL}	V _{CC} =1.65V~5.5V, I _{OH} =-100μA			0.1	V
		V _{CC} =1.65V, I _{OH} =4mA			0.45	
		V _{CC} =2.3V, I _{OH} =8mA			0.3	
		V _{CC} =3.0V, I _{OH} =16mA			0.4	
		V _{CC} =3.0V, I _{OH} =24mA			0.55	
		V _{CC} =4.5V, I _{OH} =32mA			0.55	
Input Leakage Current	I _{I(LEAK)}	V _{CC} =0V~5.5V, V _{IN} =5.5V or GND			±10	μA
Power OFF Leakage Current	I _{OFF}	V _{CC} =0V, V _{IN} or V _{OUT} =5.5V			±10	μA
Quiescent Supply Current	I _Q	V _{CC} =1.65V ~ 5.5V, V _{IN} =5.5V or GND, I _{OUT} =0			10	μA
Additional Quiescent Supply Current	ΔI _Q	V _{CC} =3V~5.5V, One input at V _{CC} -0.6V, other inputs at V _{CC} or GND			500	μA
Input Capacitance	C _{IN}	V _{CC} =3.3V, V _{IN} =V _{CC} or GND		4		pF

■ DYNAMIC CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	Conditions	MIN	TYP	MAX	UNIT
f _{clock} Clock frequency					160	MHZ
Pulse duration	t _w	V _{CC} =1.8V±0.15V	2.5			ns
		V _{CC} =2.5V±0.2V	2.5			
		V _{CC} =3.3V±0.3V	2.5			
		V _{CC} =5V±0.5V	2.5			
Setup time before CLK ↑	t _{su}	Data in high	V _{CC} =1.8V±0.15V	2.2		ns
			V _{CC} =2.5V±0.2V	1.4		
			V _{CC} =3.3V±0.3V	1.3		
			V _{CC} =5V±0.5V	1.2		
		Data in low	V _{CC} =1.8V±0.15V	2.6		
			V _{CC} =2.5V±0.2V	1.4		
			V _{CC} =3.3V±0.3V	1.3		
			V _{CC} =5V±0.5V	1.2		
Hold time ,data after CLK ↑	t _h	V _{CC} =1.8V±0.15V,	0.3		ns	
		V _{CC} =2.5V±0.2V	0.4			
		V _{CC} =3.3V±0.3V	1			
		V _{CC} =5V±0.5V	0.5			

■ SWITCHING CHARACTERISTIC (Input: $t_r, t_f \leq 2.5\text{ns}$; $\text{PRR} \leq 1\text{MHz}$)

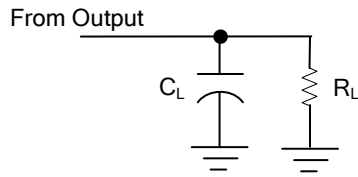
See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum clock pulse frequency	f_{MAX}	$V_{\text{CC}} = 1.65\text{V} \sim 5.5\text{V}$	160			MHz
Propagation delay from input (CLK) to output(Q)	$t_{\text{PLH}}/t_{\text{PHL}}$	$V_{\text{CC}} = 1.65\text{V} \sim 1.95\text{V}, \text{CL} = 15\text{pF}$	2.5		9.1	ns
		$V_{\text{CC}} = 2.3\text{V} \sim 2.7\text{V}, \text{CL} = 15\text{pF}$	1.2		6.0	
		$V_{\text{CC}} = 3.0\text{V} \sim 3.6\text{V}, \text{CL} = 15\text{pF}$	1.0		4.0	
		$V_{\text{CC}} = 4.5\text{V} \sim 5.5\text{V}, \text{CL} = 15\text{pF}$	0.8		3.8	
Propagation delay from input (CLK) to output(Q)	$t_{\text{PLH}}/t_{\text{PHL}}$	$V_{\text{CC}} = 1.65\text{V} \sim 1.95\text{V}, \text{CL} = 30\text{pF}$	3.9		9.9	ns
		$V_{\text{CC}} = 2.3\text{V} \sim 2.7\text{V}, \text{CL} = 30\text{pF}$	2.0		7.0	
		$V_{\text{CC}} = 3.0\text{V} \sim 3.6\text{V}, \text{CL} = 50\text{pF}$	1.7		5.0	
		$V_{\text{CC}} = 4.5\text{V} \sim 5.5\text{V}, \text{CL} = 50\text{pF}$	1.0		4.5	

■ OPERATING CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Cpd	$V_{\text{CC}} = 3.3\text{V}, f = 10\text{MHz}$		27		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

Fig.1 Load circuitry for switching times.

V_{CC}	V_{IN}	t_R, t_F	V_M	C_L	R_L
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	15pF	1MΩ
				30pF	1KΩ
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	15pF	1MΩ
				30pF	500Ω
3.3V±0.3V	3 V	≤2.5ns	1.5V	15pF	1MΩ
				50pF	500Ω
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	15pF	1MΩ
				50pF	500Ω

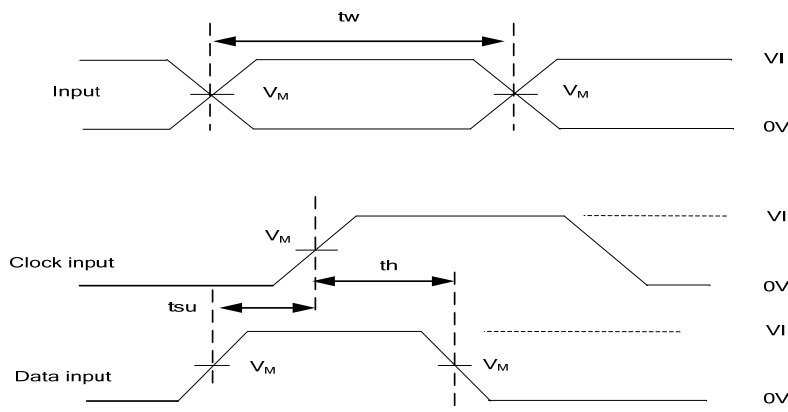
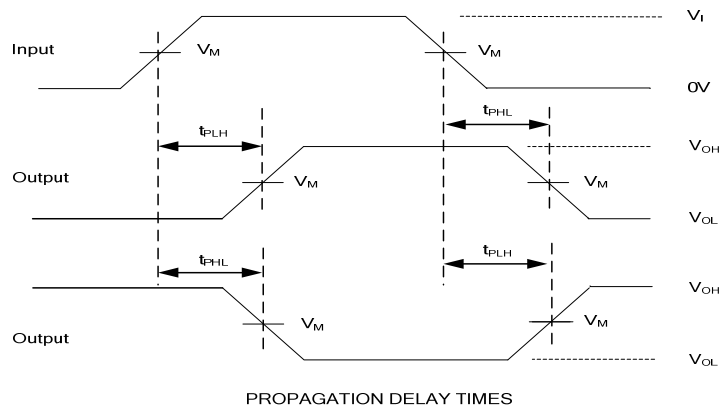


Fig. 2 Propagation delay from input to output and input voltage waveforms.

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, $Z_o = 50\Omega$.

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