



## U74LVC273

CMOS IC

### OCTAL D-TYPE FLIP-FLOP WITH CLEAR ; POSITIVE-EDGE TRIGGER

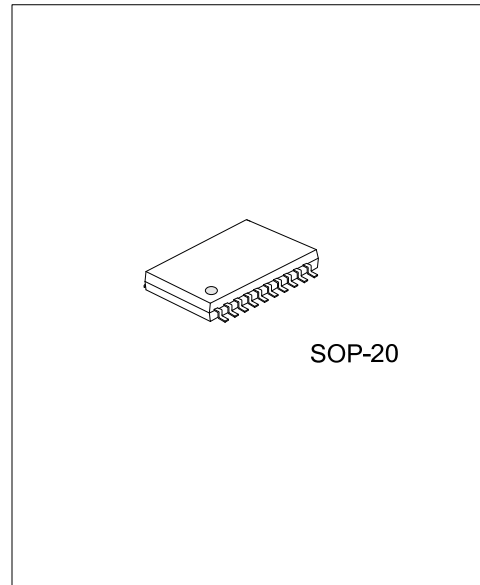
#### DESCRIPTION

The **U74LVC273** is a octal D-type Flip-Flop with 3-state outputs, and it has 8 channels with individual D inputs and Q outputs.

The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding output (Qn) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a Low voltage level on the  $\overline{MR}$  input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.



#### FEATURES

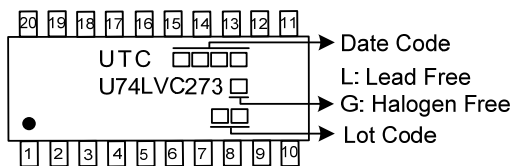
- \* Operate From 1.2V to 3.6V
- \* Inputs Accept Voltages to 5.5 V
- \* Max tpd of 6.8 ns at 3.3 V
- \* I<sub>off</sub> Supports Partial-Power-Down Mode Operation

#### ORDERING INFORMATION

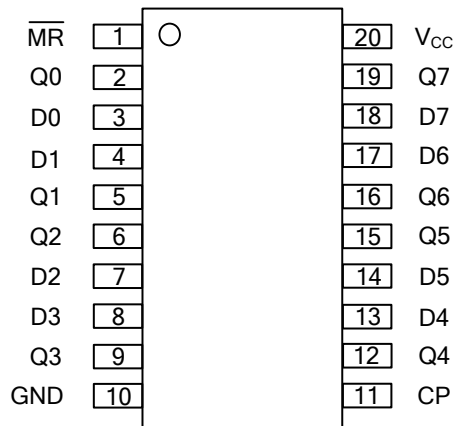
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC273L-S20-R	U74LVC273G-S20-R	SOP-20	Tape Reel

<p>U74LVC273G-S20-R</p> <ul style="list-style-type: none"> <li>(1) Packing Type</li> <li>(2) Package Type</li> <li>(3) Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) R: Tape Reel</li> <li>(2) S20: SOP-20</li> <li>(3) G: Halogen Free and Lead Free, L: Lead Free</li> </ul>
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#### MARKING



■ PIN CONFIGURATION



■ FUNCTION TABLE

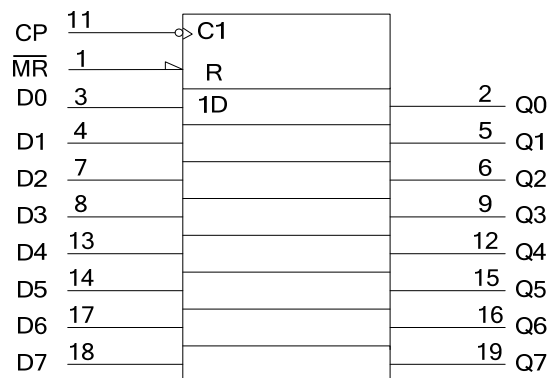
MODE	INPUTS			OUTPUT
	INPUT( $\overline{MR}$ )	CP	Dn	Qn
Reset (clear)	L	X	X	L
Load " 1 "	H	↑	h	H
Load " 0 "	H	↑	l	L

H = High voltage level ; L = Low voltage level ; X = Don't care ; ↑ = LOW-to-HIGH clock transition

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

■ LOGIC SYMBOL



## ■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	$V_{CC}$		-0.5 ~ +6.5	V
Input Voltage (Note 2)	$V_{IN}$		-0.5 ~ +6.5	V
Output Voltage	$V_{OUT}$	Output in the high or low state	-0.5 ~ $V_{CC}+0.5$	V
Continuous $V_{CC}$ or GND Current	$I_{CC}$		±100	mA
Continuous Output Current	$I_{OUT}$	$V_{OUT}=0V \sim V_{CC}$	±50	mA
Input Clamp Current	$I_{IK}$	$V_{IN}<0V$	-50	mA
Output Clamp Current	$I_{OK}$	$V_{OUT}>V_{CC}$ or $V_{OUT}<0V$	50	mA
Storage Temperature Range	$T_{STG}$		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC}$		1.65		3.6	V
		Functional	1.2			V
Input Voltage	$V_{IN}$		0		5.5	V
Output Voltage	$V_{OUT}$		0		$V_{CC}$	V
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=1.65V \sim 2.7V$	0		20	ns/V
		$V_{CC}=2.7V \sim 3.6V$	0		10	ns/V
Operating Temperature	$T_A$		-40		+85	°C

## ■ ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	$V_{IH}$	$V_{CC}=1.2V$	1.08			V
		$V_{CC}=1.8V \pm 0.15V$	$0.65 \times V_{CC}$			V
		$V_{CC}=2.5V \pm 0.2V$	1.7			V
		$V_{CC}=3.3V \pm 0.3V$	2.0			V
Low-level Input Voltage	$V_{IL}$	$V_{CC}=1.2V$			0.12	V
		$V_{CC}=1.8V \pm 0.15V$			$0.35 \times V_{CC}$	V
		$V_{CC}=2.5V \pm 0.2V$			0.7	V
		$V_{CC}=3.3V \pm 0.3V$			0.8	V
High-Level Output Voltage	$V_{OH}$	$V_{CC}=1.65V \sim 3.6V, I_{OH}=-100\mu A$	$V_{CC}-0.2$			V
		$V_{CC}=1.65V, I_{OH}=-4mA$	1.2			V
		$V_{CC}=2.3V, I_{OH}=-8mA$	1.8			V
		$V_{CC}=2.7V, I_{OH}=-12mA$	2.2			V
		$V_{CC}=3.0V$				
		$I_{OH}=-18mA$	2.4			V
		$I_{OH}=-24mA$	2.2			V
Low-Level Output Voltage	$V_{OL}$	$V_{CC}=1.65V \sim 3.6V, I_{OL}=100\mu A$			0.2	V
		$V_{CC}=1.65V, I_{OL}=4mA$			0.45	V
		$V_{CC}=2.3V, I_{OL}=8mA$			0.6	V
		$V_{CC}=2.7V, I_{OL}=12mA$			0.4	V
		$V_{CC}=3.0V, I_{OL}=24mA$			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=3.6V, V_{IN}=5.5V$ or GND		±0.1	±5	μA
Quiescent Supply Current	$I_{CC}$	$V_{CC}=3.6V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0A$		0.1	10	μA
Additional Quiescent Supply Current Per Input Pin	$\Delta I_{CC}$	$V_{CC}=2.7V \sim 3.6V, V_{CC}-0.6V, I_{OUT}=0A$		5.0	500	μA
Input Capacitance	$C_I$	$V_{CC}=0V \sim 3.6V, V_{IN}=V_{CC}$ or GND		5.0		pF

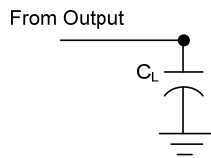
■ SWITCHING CHARACTERISTICS (T<sub>A</sub> =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Clock Pulse Frequency	f <sub>MAX</sub>	V <sub>CC</sub> =1.8V±0.15V	80			MHz
		V <sub>CC</sub> =2.5V±0.2V	100			MHz
		V <sub>CC</sub> =2.7V	150			MHz
		V <sub>CC</sub> =3.3V±0.3V	150	230		MHz
Propagation delay from input (CP) to output(Qn)	t <sub>PD</sub>	V <sub>CC</sub> =1.2V		18		ns
		V <sub>CC</sub> =1.8V±0.15V	2.5	9.7	19.2	ns
		V <sub>CC</sub> =2.5V±0.2V	1.8	4.9	9.9	ns
		V <sub>CC</sub> =2.7V	1.5	4.5	8.4	ns
Propagation delay from input (MR ) to output(Qn)	t <sub>PHL</sub>	V <sub>CC</sub> =1.2V		18		ns
		V <sub>CC</sub> =1.8V±0.15V	2.4	10.2	20.4	ns
		V <sub>CC</sub> =2.5V±0.2V	1.7	5.2	10.5	ns
		V <sub>CC</sub> =2.7V	1.5	4.7	8.9	ns
Pulse Width Clock HIGH or LOW	t <sub>w</sub>	V <sub>CC</sub> =1.8V±0.15V	6.0			ns
		V <sub>CC</sub> =2.5V±0.2V	5.0			ns
		V <sub>CC</sub> =2.7V	5.0	1.8		ns
		V <sub>CC</sub> =3.3V±0.3V	4.0	1.2		ns
Pulse Width Master Reset LOW	t <sub>w</sub>	V <sub>CC</sub> =1.8V±0.15V	6.0			ns
		V <sub>CC</sub> =2.5V±0.2V	5.0			ns
		V <sub>CC</sub> =2.7V	5.0	1.7		ns
		V <sub>CC</sub> =3.3V±0.3V	4.0	1.2		ns
Recovery Time MR to CP	t <sub>REC</sub>	V <sub>CC</sub> =1.8V±0.15V	2.0			ns
		V <sub>CC</sub> =2.5V±0.2V	2.0			ns
		V <sub>CC</sub> =2.7V	2.0	-1.0		ns
		V <sub>CC</sub> =3.3V±0.3V	2.0	-1.0		ns
Setup Time Dn to CP	t <sub>SU</sub>	V <sub>CC</sub> =1.8V±0.15V	5.0			ns
		V <sub>CC</sub> =2.5V±0.2V	3.5			ns
		V <sub>CC</sub> =2.7V	3.0	1.0		ns
		V <sub>CC</sub> =3.3V±0.3V	1.0	0.0		ns
Hold Time Dn to CP	t <sub>H</sub>	V <sub>CC</sub> =1.8V±0.15V	3.0			ns
		V <sub>CC</sub> =2.5V±0.2V	2.5			ns
		V <sub>CC</sub> =2.7V	2.0	-2.0		ns
		V <sub>CC</sub> =3.3V±0.3V	1.0	0.0		ns
Propagation delay	t <sub>SK(O)</sub>	V <sub>CC</sub> =3.3V±0.3V			1.0	ns

■ OPERATING CHARACTERISTICS (f=10MHz, T<sub>A</sub> =25°C , unless otherwise specified)

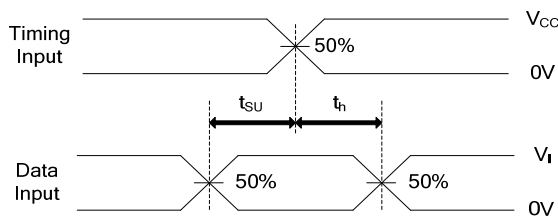
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C <sub>PD</sub>	V <sub>CC</sub> =1.8V±0.15V		14		pF
		V <sub>CC</sub> =2.5V±0.2V		17.7		pF
		V <sub>CC</sub> =3.3V±0.3V		21		pF

## ■ TEST CIRCUIT AND WAVEFORMS

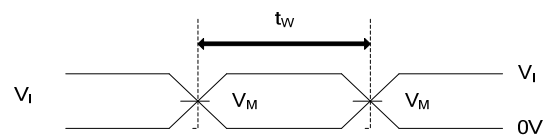


TEST CIRCUIT

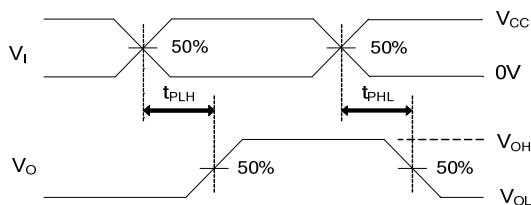
$V_{CC}$	INPUTS		$L_{LOAD}$		$V_{EXT}$		
	$V_{IN}$	$t_R/t_F$	$C_L$	$R_L$	$t_{PLH}/t_{PHL}$	$t_{PLZ}/t_{PZL}$	$t_{PHZ}/t_{PZH}$
1.2V	$V_{CC}$	$\leq 2ns$	30pF	1K $\Omega$	OPEN	$2 \times V_{CC}$	GND
1.8V $\pm$ 0.15V	$V_{CC}$	$\leq 2ns$	30pF	1K $\Omega$	OPEN	$2 \times V_{CC}$	GND
2.5V $\pm$ 0.2V	$V_{CC}$	$\leq 2ns$	30pF	500 $\Omega$	OPEN	$2 \times V_{CC}$	GND
2.7V	2.7V	$\leq 2.5ns$	50pF	500 $\Omega$	OPEN	$2 \times V_{CC}$	GND
3.3V $\pm$ 0.3V	2.7V	$\leq 2.5ns$	50pF	500 $\Omega$	OPEN	$2 \times V_{CC}$	GND



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATION



PROPAGATION DELAY TIMES

Notes: 1.  $C_L$  includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10MHz,  $Z_o = 50\Omega$ .

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