



## U74LVX4052

CMOS IC

### Dual 4-Channel Analog Multiplexer/Demultiplexer

#### DESCRIPTION

The **U74LVX4052** is a high speed, low-voltage drive analog multiplexer/demultiplexer using silicon gate CMOS technology. In 3V and 5V systems these can achieve high-speed operation with the low power dissipation that is a feature of CMOS.

The **U74LVX4052** offer analog/digital signal selection as well as mixed signals with a 4-Channel×2 configuration.

The switches for each channel are turned on by the control pin digital signals.

Although the control signal logical amplitude ( $V_{CC}$ -GND) is small, the device can perform large-amplitude ( $V_{CC}$ - $V_{EE}$ ) signal switching.

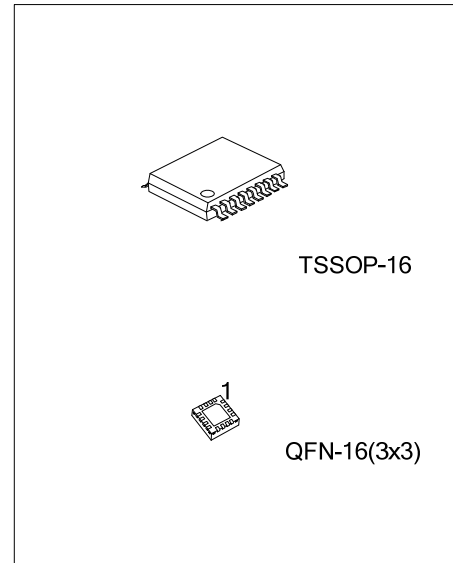
For example, if  $V_{CC}=3V$ ,  $GND=0V$  and  $V_{EE}=-3V$ , signals between -3V and +3V can be switched from the logical circuit using a signal 3V power supply.

All input pins are equipped with a newly developed input protection circuit that avoids the need for a diode on the plus side (forward side from the input to the  $V_{CC}$ ). As a result, for example, 5V signals can be permitted on the inputs even when the power supply voltage to the circuits is off. As a result of this input power protection, the **U74LVX4052** can be used in a variety of applications, including in the system which has two power supplies, and in battery backup circuits.

#### FEATURES

- \* Low ON resistance:  $R_{ON}=22\Omega$ (Typ.)( $V_{CC}-V_{EE}=3V$ )
- \*  $R_{ON}=15\Omega$ (Typ.)( $V_{CC}-V_{EE}=6V$ )
- \* High Speed:  $t_{pd}=3ns$  (Typ.)( $V_{CC}=3V$ )
- \* Low power Dissipation:  $I_{CC}=4\mu A$  (Max.)( $T_A=25^\circ C$ )

- \* Input level:  $V_{IL}=0.8V$ (Max.)( $V_{CC}=3V$ )
- $V_{IH}=2.0V$ (Min.)( $V_{CC}=3V$ )
- \* Power down protection is provided on all control inputs
- \* Pin and function compatible with U74HC4052

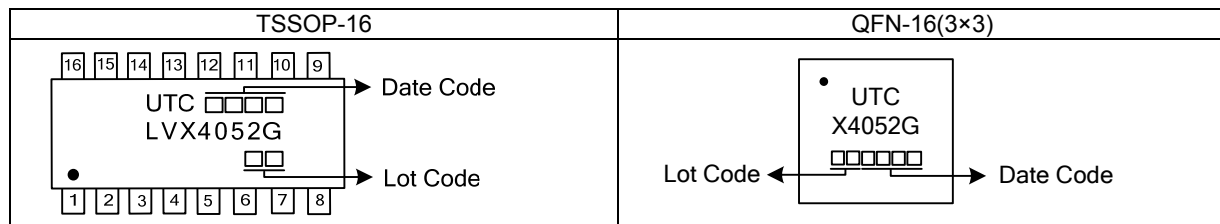


#### ORDERING INFORMATION

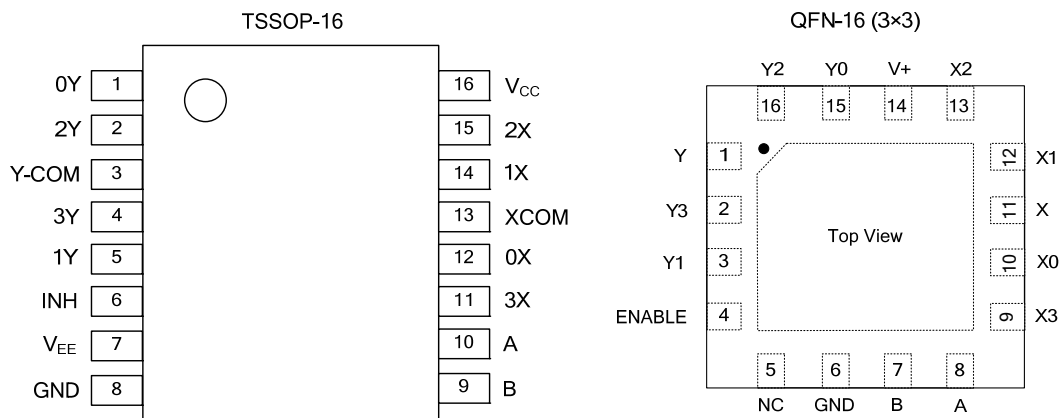
Ordering Number	Package	Packing
U74LVX4052G-P16-R	TSSOP-16	Tape Reel
U74LVX4052G-Q16-3030-R	QFN-16(3×3)	Tape Reel

<p>U74LVX4052G-P16-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) P16: TSSOP-16, Q16-3030: QFN-16(3×3) (3) G: Halogen Free and Lead Free</p>
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MARKING



PIN CONFIGURATION

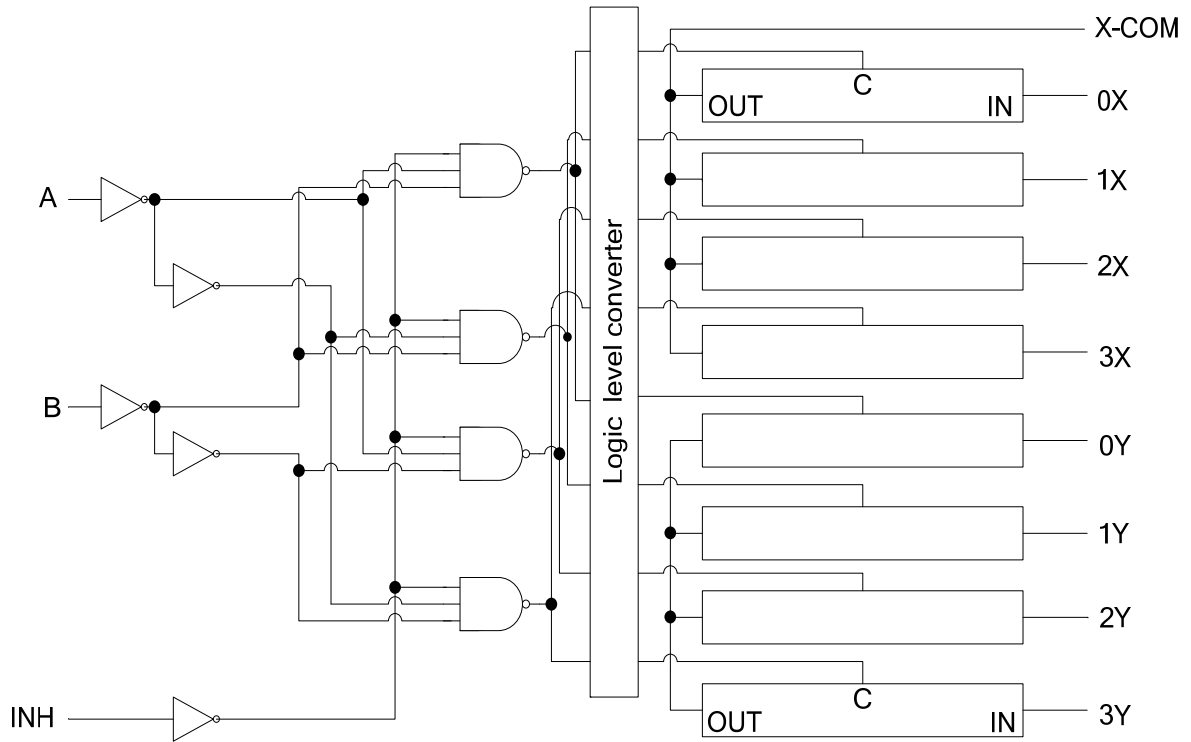


FUNCTION TABLE

CONTROL INPUTS			"ON" Channel
INH	B	A	LVX4052
L	L	L	0X,0Y
L	L	H	1X,1Y
L	H	L	2X,2Y
L	H	H	3X,3Y
H	X	X	None

Note: H: HIGH voltage level; L: LOW voltage level; X: Don't care

■ LOGIC DIAGRAM (positive logic)



### ■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Power Supply Voltage		$V_{CC}$	-0.5 ~ +7.0	V
		$V_{CC} \sim V_{EE}$	-0.5 ~ +7.0	
Control Input Voltage		$V_{IN}$	-0.5 ~ +7.0	V
Switch I/O voltage		$V_{I/O}$	$V_{EE} - 0.5 \sim V_{CC} + 0.5$	V
Input diode current		$I_{IK}$	-20	mA
I/O diode Current		$I_{IOK}$	±20	mA
Switch through current		$I_T$	±25	mA
DC Vcc or ground current		$I_{CC}$	±50	mA
Power dissipation	TSSOP-16	$P_D$	450	mW
	QFN-16(3×3)		500	mW
Operating Temperature		$T_{OPR}$	-40 ~ +85	°C
Storage Temperature		$T_{STG}$	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.  
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

### ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Voltage	$V_{CC}$		2.0		6.0	V
	$V_{EE}$		-4		0	
	$V_{CC} \sim V_{EE}$		2		6	
Input Voltage	$V_{IN}$		0		6	V
Switch I/O Voltage	$V_{I/O}$		$V_{EE}$		$V_{CC}$	V
Input Rise and Fall time	dt/dv	$V_{CC} = 3.3V \pm 0.3$	0		100	ns/V
		$V_{CC} = 5V \pm 0.5$	0		20	

■ DC ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage	High-level	V <sub>IH</sub>	V <sub>CC</sub> =2V	1.5			V
			V <sub>CC</sub> =3V	2.0			
			V <sub>CC</sub> =4.5V	3.15			
			V <sub>CC</sub> =6V	4.2			
	Low-level	V <sub>IL</sub>	V <sub>CC</sub> =2V			0.5	
			V <sub>CC</sub> =3V			0.8	
			V <sub>CC</sub> =4.5V			1.35	
			V <sub>CC</sub> =6V			1.8	
ON resistance	R <sub>ON</sub>	V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> V <sub>I/O</sub> =V <sub>CC</sub> to V <sub>EE</sub> I <sub>I/O</sub> =2mA	V <sub>CC</sub> =2V, V <sub>EE</sub> =GND		200		Ω
			V <sub>CC</sub> =3V, V <sub>EE</sub> =GND		45	86	
			V <sub>CC</sub> =4.5V, V <sub>EE</sub> =GND		24	37	
			V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		17	26	
		V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> V <sub>I/O</sub> =V <sub>CC</sub> or V <sub>EE</sub> I <sub>I/O</sub> =2mA	V <sub>CC</sub> =2V, V <sub>EE</sub> =GND		28	73	
			V <sub>CC</sub> =3V, V <sub>EE</sub> =GND		22	38	
			V <sub>CC</sub> =4.5V, V <sub>EE</sub> =GND		17	27	
			V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		15	24	
Difference of ON resistance between switches	ΔR <sub>ON</sub>	V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> V <sub>I/O</sub> =V <sub>CC</sub> to V <sub>EE</sub> I <sub>I/O</sub> =2mA	V <sub>CC</sub> =2V, V <sub>EE</sub> =GND		10	25	Ω
			V <sub>CC</sub> =3V, V <sub>EE</sub> =GND		5	15	
			V <sub>CC</sub> =4.5V, V <sub>EE</sub> =GND		5	13	
			V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		5	10	
Input/Output Leakage Current (switch off)	I <sub>OFF</sub>	V <sub>OS</sub> =V <sub>CC</sub> or GND, V <sub>IS</sub> =GND or V <sub>CC</sub> , V <sub>IN</sub> =V <sub>IH</sub> OR V <sub>IL</sub>	V <sub>CC</sub> =3V, V <sub>EE</sub> =GND			±0.25	μA
			V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V			±0.5	
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND	V <sub>CC</sub> =3V, V <sub>EE</sub> =GND			4.0	μA
			V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V			8.0	μA
Input/Output leakage current (switch on, output open)	I <sub>IN</sub>	V <sub>OS</sub> =V <sub>CC</sub> or GND, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub>	V <sub>CC</sub> =3V, V <sub>EE</sub> =GND			±0.25	μA
			V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V			±0.5	
Control input current	I <sub>IN</sub>	V <sub>IN</sub> =V <sub>CC</sub> or GND	V <sub>CC</sub> =6V, V <sub>EE</sub> =GND			±0.1	μA

■ AC ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C, Input t<sub>R</sub>/t<sub>F</sub> =3ns, GND=0V, C<sub>L</sub>=50pF)

See Fig. 1 , Fig. 2 and Fig. 3 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase difference between input and output	t <sub>PLH</sub> /t <sub>PHL</sub>	V <sub>CC</sub> =2V, V <sub>EE</sub> =GND		3.2	6.0	ns
		V <sub>CC</sub> =3V, V <sub>EE</sub> =GND		1.8	3.0	
		V <sub>CC</sub> =4.5V, V <sub>EE</sub> =GND		1.3	1.8	
		V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		1.1	1.3	
Output enable time (Note 1)	t <sub>PZL</sub> /t <sub>PZH</sub>	V <sub>CC</sub> =2V, V <sub>EE</sub> =GND		9	17	ns
		V <sub>CC</sub> =3V, V <sub>EE</sub> =GND		5.7	9	
		V <sub>CC</sub> =4.5V, V <sub>EE</sub> =GND		4.5	6	
		V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		5.8	8	
Output disable time (Note 1)	t <sub>PLZ</sub> /t <sub>PHZ</sub>	V <sub>CC</sub> =2V, V <sub>EE</sub> =GND		13.5	21	ns
		V <sub>CC</sub> =3V, V <sub>EE</sub> =GND		11.3	15	
		V <sub>CC</sub> =4.5V, V <sub>EE</sub> =GND		10.3	12	
		V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		10.9	13	
Control input capacitance (Note 2)	C <sub>IN</sub>			5	10	pF
COMMON terminal capacitance (Note 2)	C <sub>IS</sub>	V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		9	20	pF
SWITCH terminal capacitance (Note 2)	C <sub>OS</sub>	V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		6	13	pF
Feedthrough capacitance (Note 2)	C <sub>IOS</sub>	V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		3	6	pF
Power dissipation capacitance (Note 3)	C <sub>PD</sub>	V <sub>CC</sub> =6V, V <sub>EE</sub> =GND		24		pF

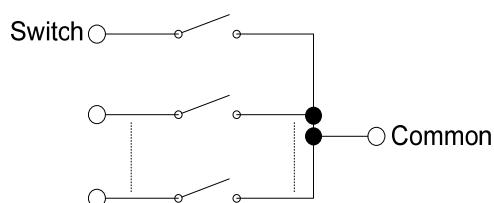
Note: 1. R<sub>L</sub>=1k

2. C<sub>IN</sub>, C<sub>IS</sub>, C<sub>OS</sub> and C<sub>IOS</sub> are guaranteed by the design.
3. CPD is defined as the value of the internal equivalent capacitance of IC which is calculated from the operating current consumption without load.  
Average operating current can be obtained by the equation.  
 $I_{CC(OPR)} = C_{PD} \times V_{CC} \times f_{IN} + V_{CC}$

■ Analog Switch CHARACTERISTICS (GND=0V, T<sub>A</sub>=25°C) (Note)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
Sine Wave Distortion	THD	R <sub>L</sub> =10k, C <sub>L</sub> =50pF, f <sub>IN</sub> =1k	V <sub>IN</sub> =2Vp-p, V <sub>CC</sub> =3V, V <sub>EE</sub> =0V		0.1		%	
			V <sub>IN</sub> =4Vp-p, V <sub>CC</sub> =4.5V, V <sub>EE</sub> =0V		0.03			
			V <sub>IN</sub> =6Vp-p, V <sub>CC</sub> =3V, V <sub>EE</sub> =-0.3V		0.02			
Frequency response (switch on)	f <sub>MAX</sub>	Adjust f <sub>IN</sub> voltage to obtain 0dBm at V <sub>OS</sub> . Increase fin frequency until dB meter reads -3dB. R <sub>L</sub> =50Ω, C <sub>L</sub> =10pF, f <sub>IN</sub> =1MHz, sine wave (Figure 4)	V <sub>CC</sub> =3V, V <sub>EE</sub> =0V		180		MHz	
			V <sub>CC</sub> =4.5V, V <sub>EE</sub> =0V		180			
			V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		180			
Feed through attenuation (switch off)		V <sub>IN</sub> is centered at (V <sub>CC</sub> -V <sub>EE</sub> )/2. Adjust input for 0dBm. R <sub>L</sub> =600Ω, C <sub>L</sub> =50pF, f <sub>IN</sub> =1MHz, sine wave (Figure 5)	V <sub>CC</sub> =3V, V <sub>EE</sub> =0V		-45		dB	
			V <sub>CC</sub> =4.5V, V <sub>EE</sub> =0V		-45			
			V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		-45			
			R <sub>L</sub> =50Ω, C <sub>L</sub> =10pF, f <sub>IN</sub> =1MHz, sine wave	V <sub>CC</sub> =3V, V <sub>EE</sub> =0V		-60		
			V <sub>CC</sub> =4.5V, V <sub>EE</sub> =0V		-60			
			V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		-60			
Crosstalk (control input to signal output)		R <sub>L</sub> =600Ω, C <sub>L</sub> =50pF, f <sub>IN</sub> =1MHz, square wave (t <sub>r</sub> =t <sub>f</sub> =6ns) (Figure 6)	V <sub>CC</sub> =3V, V <sub>EE</sub> =0V		90		mV	
			V <sub>CC</sub> =4.5V, V <sub>EE</sub> =0V		150			
			V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		120			
Crosstalk (between any switches)		Adjust V <sub>IN</sub> to obtain 0dBm at input. R <sub>L</sub> =600Ω, C <sub>L</sub> =50pF, f <sub>IN</sub> =1MHz, sine wave (Figure 7)	V <sub>CC</sub> =3V, V <sub>EE</sub> =0V		-45		dB	
			V <sub>CC</sub> =4.5V, V <sub>EE</sub> =0V		-45			
			V <sub>CC</sub> =3V, V <sub>EE</sub> =-3V		-45			

Note: These characteristics are determined by design of devices.



## ■ TEST CIRCUIT AND WAVEFORMS

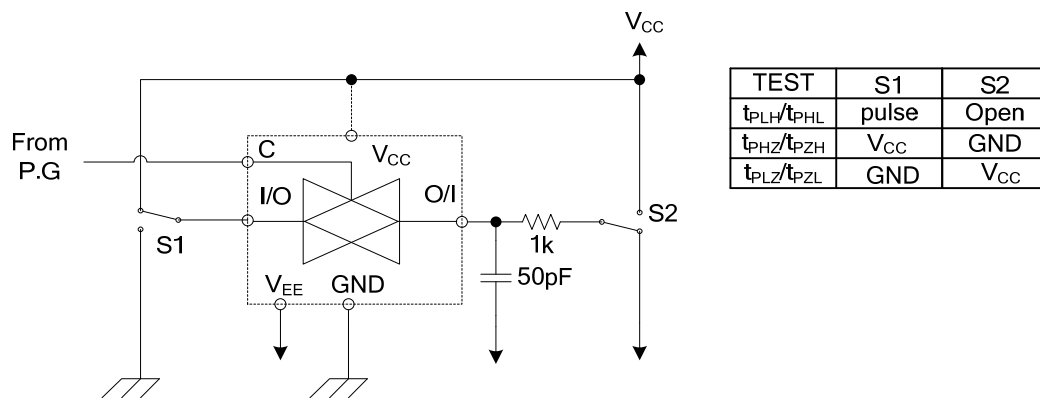


Fig. 1 Load circuitry for switching times.

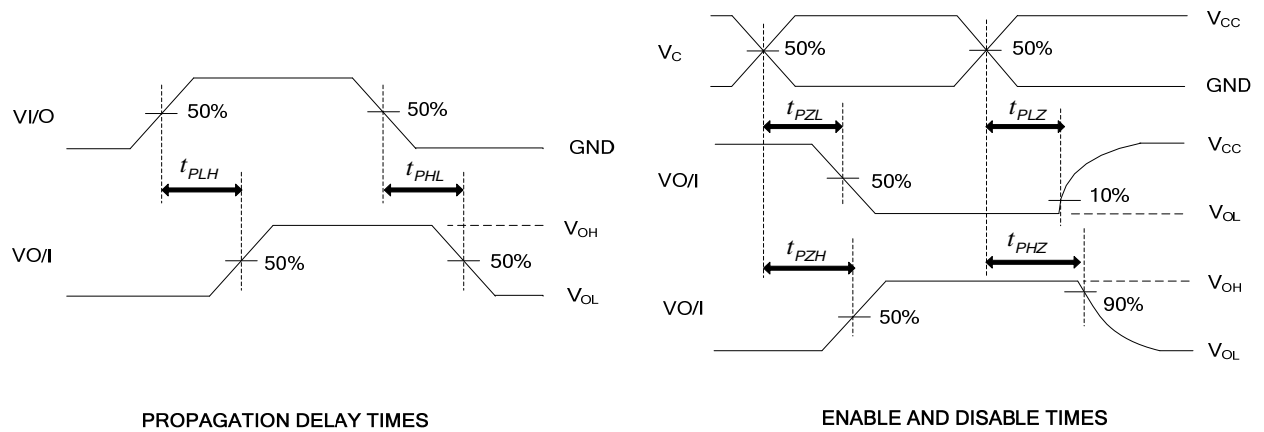


Fig. 2 Propagation delay from input to output and enable, disable times.



■ AC TEST CIRCUIT

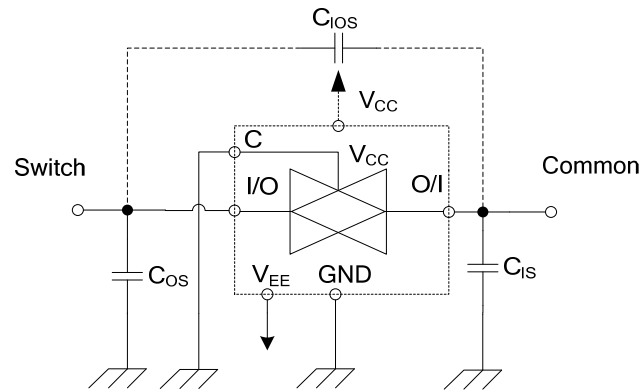


Fig. 3  $C_{1OS}$ ,  $C_{1S}$ ,  $C_{OS}$

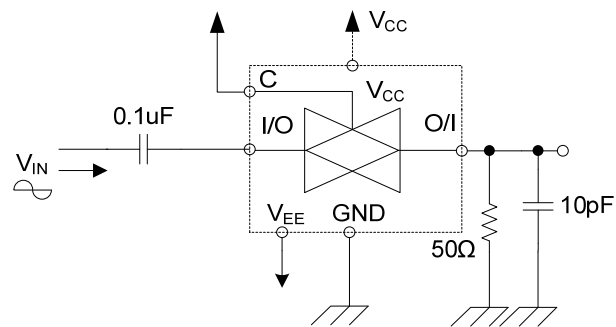


Fig. 4 Frequency Response (switch on)

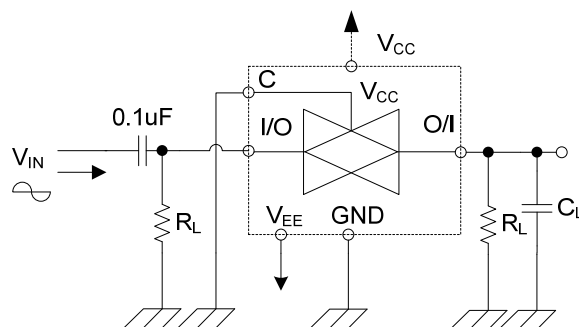


Fig. 5 Feedthrough

■ AC TEST CIRCUIT(Cont.)

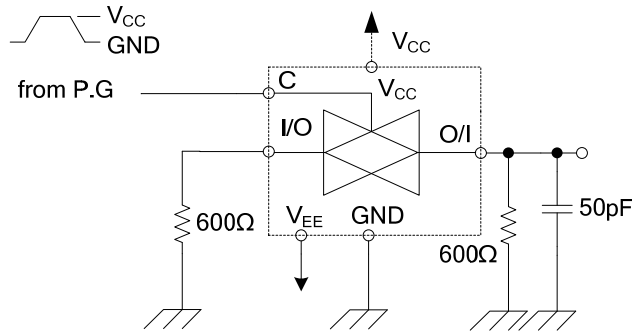


Fig. 6 Cross Talk (control input to output signal)

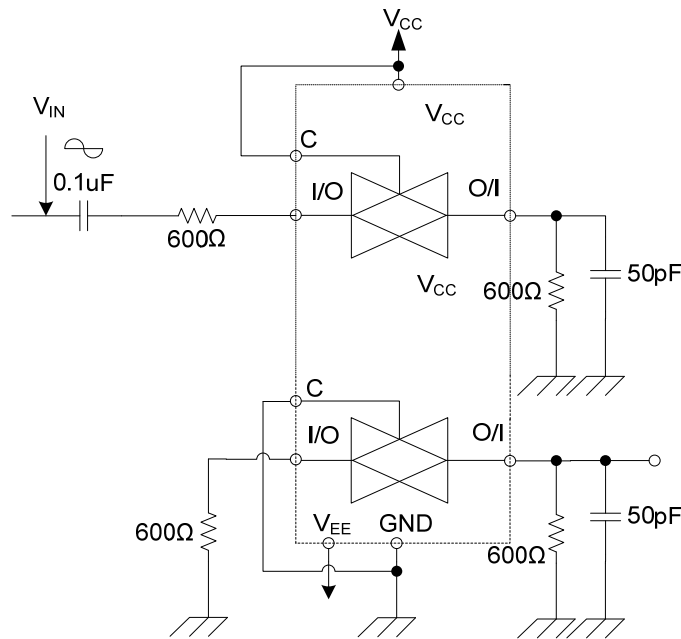


Fig. 7 Cross Talk (between any two switches)

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