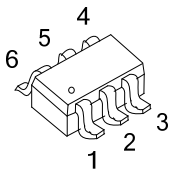
ADVANCED PWM STEP-UP DC-DC CONVERTER



SOT-26

■ DESCRIPTION

The UTC **UC3551** is a step-up DC/DC converter with high efficiency and low start-up voltage. It is operaded in stable waveforms without external compensate. This device incorporates an adaptive current mode PWM control loop in which an error amplifier, ramp generator, comparator, switch pass element and driver are included. Besides, this circuit provides a stable and high efficient operation over a wide range of load currents.

The UTC **UC3551** features high switching rate which is up to 450 KHz, making the external component counts less required. Moreover, it features 17μA low quiescent current, which makes the battery life longer. The low start-up input voltage below 1V makes UTC **UC3551** suitable for 1 to 4 battery cells applications of providing up to 300mA output current.

Two external resistors determine the value of the output voltage. The external power devices (NMOS or NPN) are derived by both internal 2A switch and driver.

The UTC **UC3551** is intended to be used in PDA, DSC, LCD Panel, RF-Tags, MP3, portable instrument and wireless equipment.

■ FEATURES

* Low Start-up Input Voltage is as Low as 1.0V
* Efficiency up to 90%
* High Supply Capability to Deliver 3.3V 100mA with 1 Alkaline Cell
* Quiescent (Switch-off) Supply Current: 17μA
* Zero Shutdown Mode Supply Current
* Fixed Switching Frequency: 450KHz
* Both Internal and External Power Switches for Maximum Flexibility

■ ORDERING INFORMATION

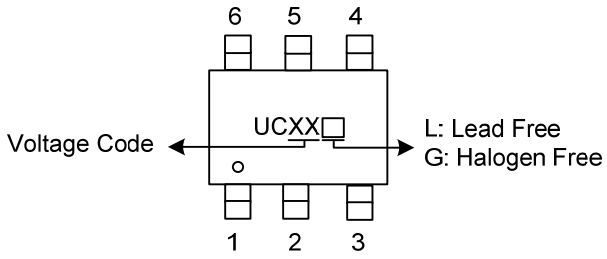
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UC3551L-xx-AG6-R	UC3551G-xx-AG6-R	SOT-26	Tape Reel

Note: xx: Output Voltage, refer to Marking Information.

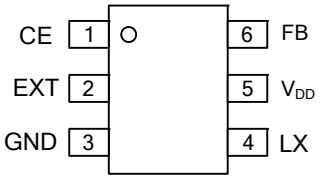
UC3551G-xx-AG6-R

(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) AF6: SOT-26
(3)Output Voltage Code	(3) xx: refer to Marking Information
(4)Green Package	(4) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
SOT-26	AD:ADJ	

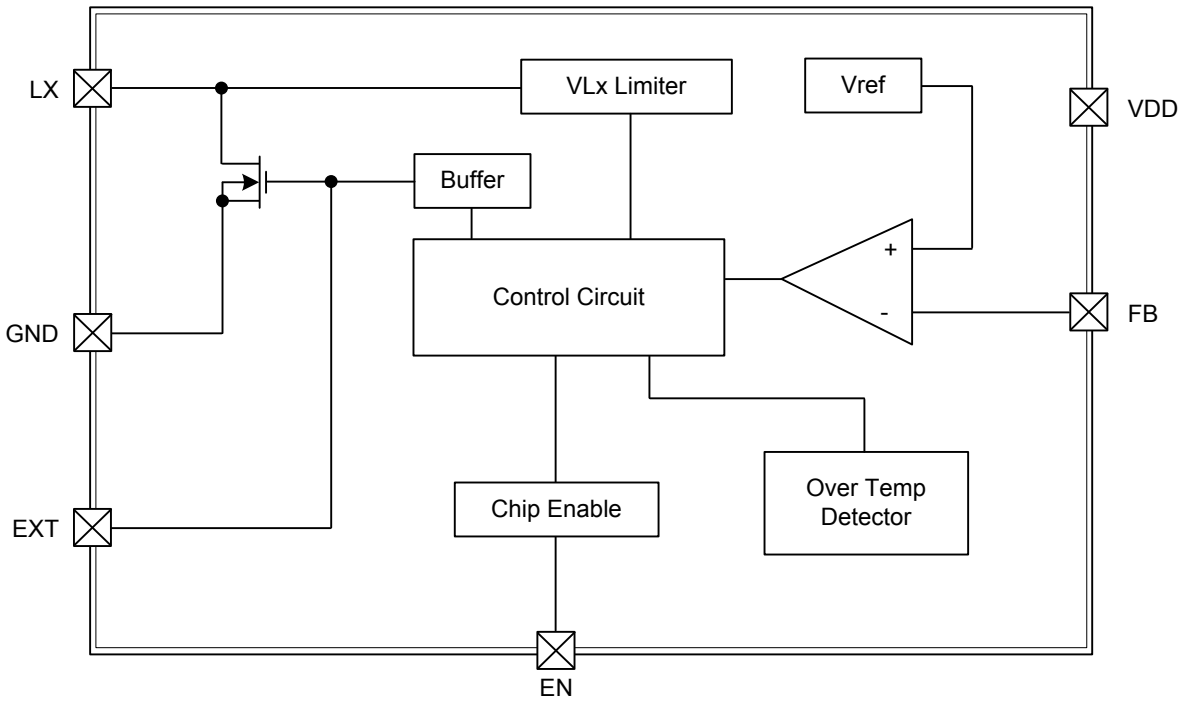
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	CE	Chip enable UC3551 gets into shutdown mode when CE pin set to low.
2	EXT	Output pin for driving external NMOS
3	GND	Ground
4	LX	Pin for switching
5	V_{DD}	Input positive power pin of UC3551
6	FB	Feedback input pin Internal reference voltage for the error amplifier is 1.25V.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{IN}	− 0.3 ~ 7	V
LX Pin Switch Voltage	V_{LX}	− 0.3 ~ (V_{DD} + 0.8)	V
Other I/O Pin Voltages		− 0.3 ~ (V_{DD} + 0.3)	V
LX Pin Switch Current	I_{LX}	2.5	A
EXT Pin Driver Current	I_{EXT}	200	mA
Operating Junction Temperature	T_{OPR}	125	°C
Storage Temperature	T_{STG}	-65~+150	°C

Notes: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Case	θ_{JC}	145	°C/W

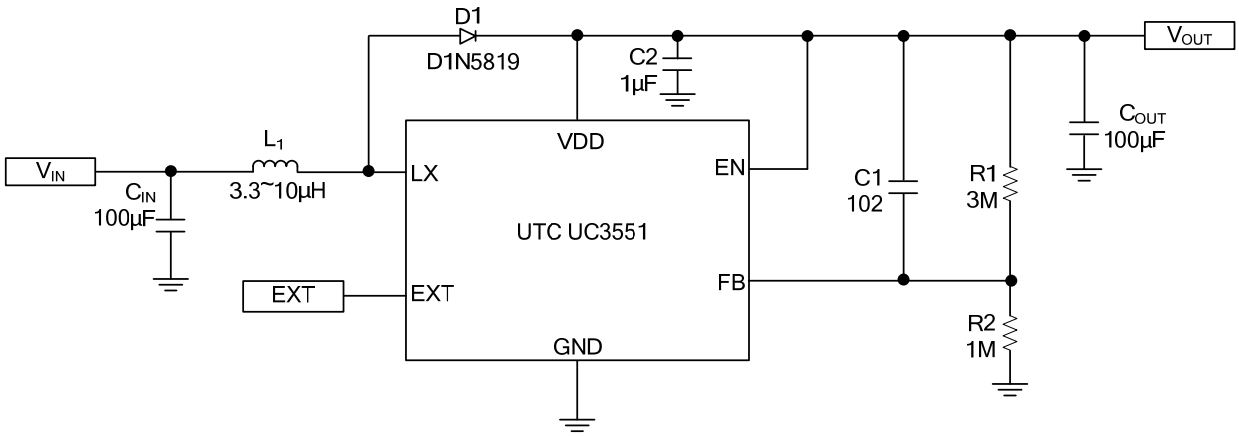
■ ELECTRICAL CHARACTERISTICS

(T_A = 25°C,V_{IN} = 1.5V, V_{DD}= 3.3V, Load Current = 0, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Start-UP Voltage	V_{ST}	I_L = 1mA		0.98	1.05	V
Operating VDD Range	V_{DD}	V_{DD} pin voltage	2		6.5 (Note)	V
No Load Current I (V_{IN})	$I_{NO\ LOAD}$	V_{IN} = 1.5V, V_{OUT} = 3.3V		75		μA
Switch-off Current I (V_{DD})	$I_{SWITCH\ OFF}$	V_{IN} = 6V		17		μA
Shutdown Current I (V_{IN})	I_{OFF}	CE Pin = 0V, V_{IN} = 4.5V		0.01	1	μA
Feedback Reference Voltage	V_{REF}	Close Loop, V_{DD} = 3.3V	1.225	1.25	1.275	V
Switching Frequency	F_S	V_{DD} = 3.3V		450		KHz
Maximum Duty	D_{MAX}	V_{DD} = 3.3V		95		%
LX ON Resistance		V_{DD} = 3.3V		0.3		Ω
Current Limit Setting	I_{LIMIT}	V_{DD} = 3.3V		2		A
EXT ON Resistance to V_{DD}		V_{DD} = 3.3V		5		Ω
EXT ON Resistance to GND		V_{DD} = 3.3V		5		Ω
Line Regulation	ΔV_{LINE}	V_{IN} = 1.5 ~ 2.5V, I_L = 1mA		10		mV/V
Load Regulation	ΔV_{LOAD}	V_{IN} = 2.5V, I_L = 1 ~ 100mA		0.25		mV/mA
CE Pin Trip Level		V_{DD} = 3.3V	0.4	0.8	1.2	V
Temperature Stability for Vout	T_s			50		ppm/°C
Thermal Shutdown	T_{SD}			165		°C
Thermal Shutdown Hysterises	ΔT_{SD}			10		°C

Note: The CE pin shall be tied to V_{DD} pin and inhibit to act the ON/OFF state whenever the V_{DD} pin voltage may reach to 5.5V or above.

■ TEST CIRCUIT



■ TYPICAL APPLICATION CIRCUIT