

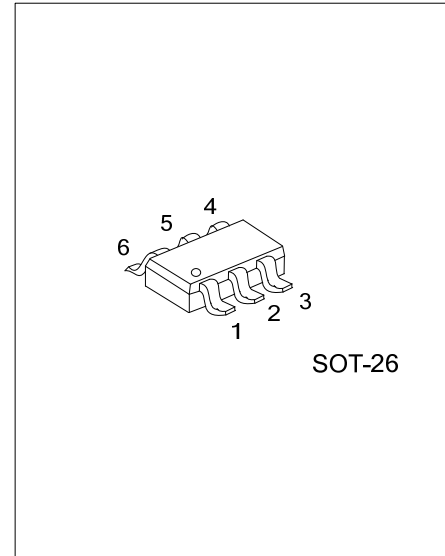


UD4N03-H

Preliminary

Power MOSFET

**4A, 30V DUAL N-CHANNEL
ENHANCEMENT MODE FIELD
EFFECT TRANSISTOR**



■ DESCRIPTION

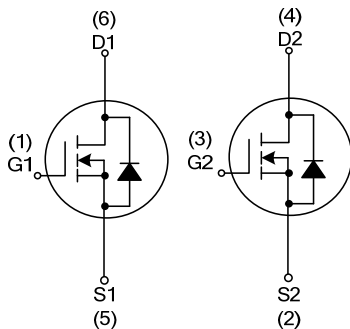
The UTC **UD4N03-H** is a dual N-Channel enhancement mode field effect transistor, it uses UTC's advanced technology to provide customers with a minimum on-state resistance and low gate charge, etc.

The UTC **UD4N03-H** is suitable for use as a load switch or in PWM applications.

■ FEATURES

- * $R_{DS(ON)} < 38\text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=3.5\text{A}$
- $R_{DS(ON)} < 72\text{ m}\Omega$ @ $V_{GS}=4.5\text{V}$, $I_D=2.5\text{A}$
- * Low gate charge

■ SYMBOL



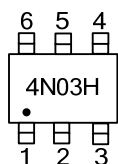
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment						Packing
Lead Free	Halogen Free		1	2	3	4	5	6	
UD4N03L-AG6-R	UD4N03G-AG6-R	SOT-26	G1	S2	G2	D2	S1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UD4N03G-AG6-R</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) R: Tape Reel</p> <p>(2) AG6: SOT-26</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current	I_D	4	A
Pulsed Drain Current (Note 2)	I_{DM}	16	A
Peak Diode Recovery dv/dt (Note 4)	dv/dt	1.7	V/ns
Power Dissipation	P_D	1.14	W
Junction Temperature	T_J	$-55 \sim +150$	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	$-55 \sim +150$	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $I_{SD} \leq 4.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J = 25^{\circ}\text{C}$.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	150	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	80	$^{\circ}\text{C}/\text{W}$

Note: Repetitive Rating: Pulse width limited by maximum junction temperature.

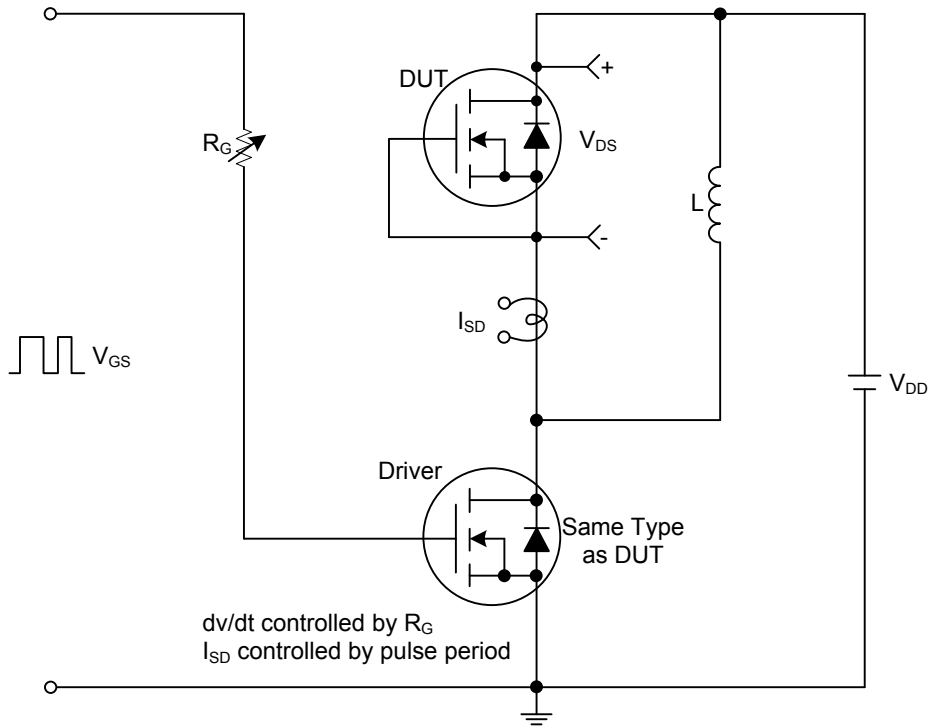
■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-Source Leakage Current	I_{GSS}	Forward $V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$			+100	nA
		Reverse $V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0		3.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=3.5\text{A}$			38	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=2.5\text{A}$			72	m Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1\text{MHz}$		200		pF
Output Capacitance	C_{OSS}			37		pF
Reverse Transfer Capacitance	C_{RSS}			32		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $I_D=1.0\text{A}$ $I_G=100\mu\text{A}$		13		nC
Gate to Source Charge	Q_{GS}			0.8		nC
Gate to Drain Charge	Q_{GD}			1.4		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $I_D=1.0\text{A}$ $R_G=25\Omega$		22		ns
Rise Time	t_R			30		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			98		ns
Fall-Time	t_F			70		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				4	A
Maximum Body-Diode Pulsed Current	I_{SM}				16	A
Diode Forward Voltage	V_{SD}	$I_S=3.5\text{A}$, $V_{GS}=0\text{V}$			1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F=4.0\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		780		ns
Body Diode Reverse Recovery Charge	Q_{rr}			2.23		μC

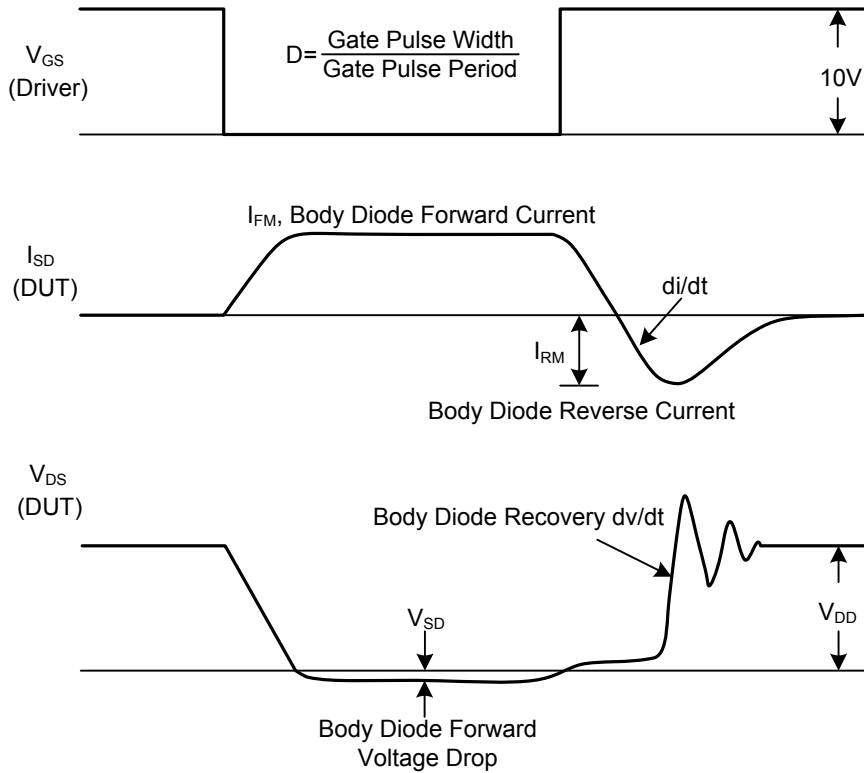
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS



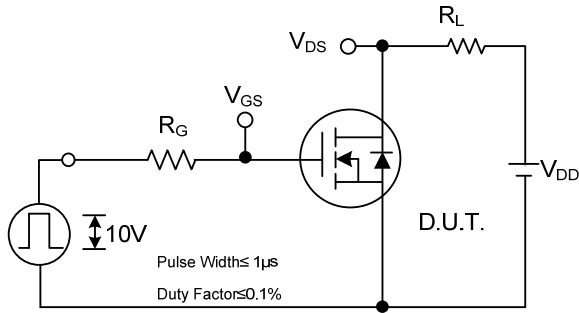
Peak Diode Recovery dv/dt Test Circuit



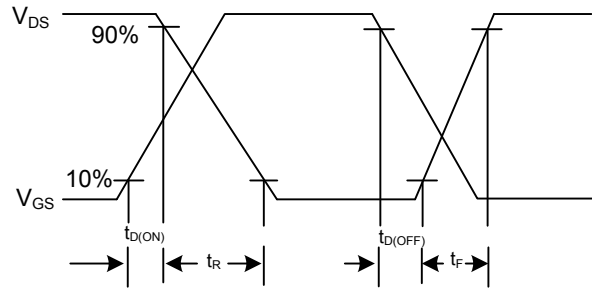
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

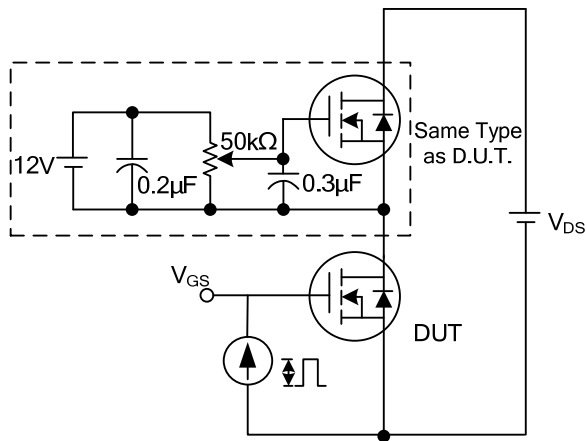
■ TEST CIRCUITS AND WAVEFORMS



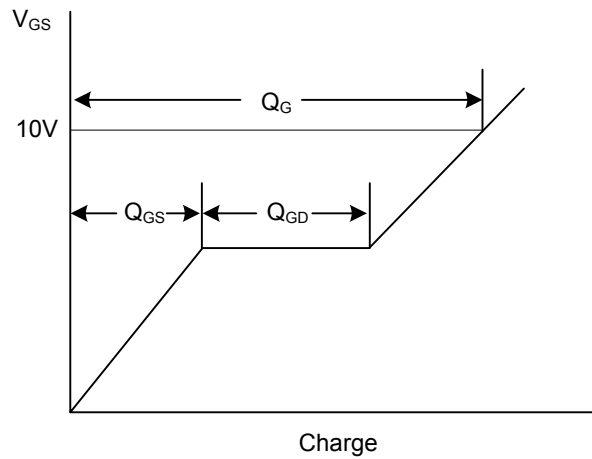
Switching Test Circuit



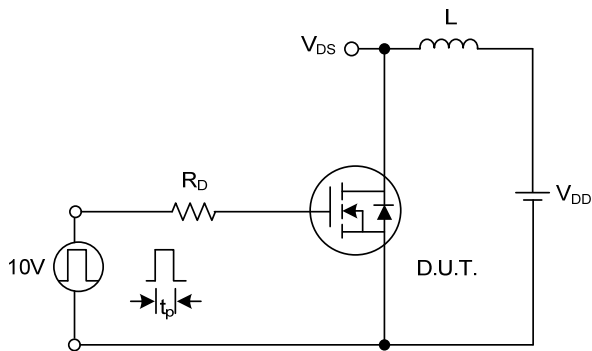
Switching Waveforms



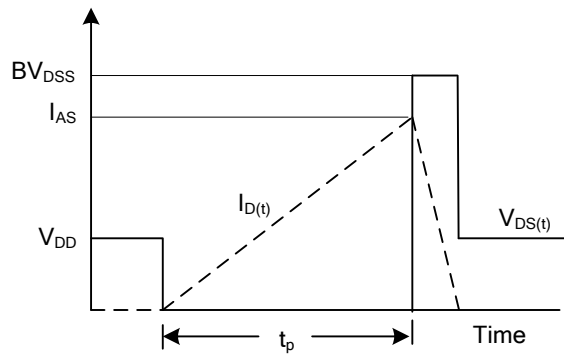
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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