# UNISONIC TECHNOLOGIES CO., LTD

## UIC809

*CMOS IC*

# MICROPROCESSOR RESET CIRCUITS



SOT-23-3
(JEDEC TO-236)

■ **DESCRIPTION**

The UTC **UIC809** series are resetting circuits which can monitor power supplies especially in microprocessor based systems.

In normal operation, the UTC **UIC809** series can assert a reset under any of the following situation: the power supply drops below a designated reset threshold level (which is available for 3V or 3.3V or 5V system) is forced low.

There is an internal active low $\overline{RESET}$ output which has already been guaranteed to remain asserted for at 140ms least while $V_{CC}$ rises above the designed threshold level.

■ **FEATURES**

* Voltage monitor for 3V or 3.3V or 5V power supplies
* Valid $\overline{RESET}$ remains with $V_{CC}$ as low as 1V
* Typical supply current: 5µA
* Fixed 140ms minimum reset pulse width
* With Manual reset input
* Push-Pull $\overline{RESET}$ Active Low Output

■ **ORDERING INFORMATION**

| Ordering Number | | Package | Pin Assignment | | | Packing |
|---|---|---|---|---|---|---|
| Lead Free | Halogen Free | | 1 | 2 | 3 | |
| UIC809Lx-AE2-3-R | UIC809G-x-AE2-3-R | SOT-23-3 | GND | $\overline{RESET}$ | $V_{CC}$ | Tape Reel |

Note: Pin Assignment :    x: Output Voltage, refer to Marking Information.

UIC809G-x-AE2-3-R

- (1) Packing Type
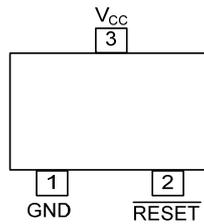- (2) Pin Assignment
- (3) Package Type
- (4) Output Voltage Code
- (5) Green Package

(1) R: Tape Reel
(2) refer to Pin Assignment
(3) AE2: SOT-23-3
(4) x: Refer to Marking Information
(5) G: Halogen Free and Lead Free, L: Lead Free

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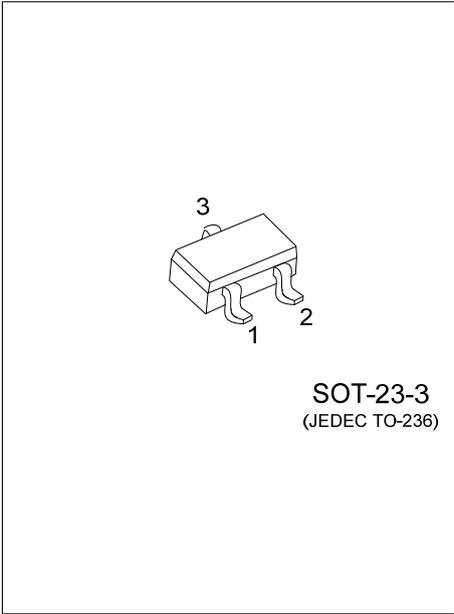
■ **MARKING INFORMATION**

| PACKAGE | VOLTAGE CODE | MARKING |
|---|---|---|
| SOT-23-3 | B : 2.93V | <br>3<br><br>UX□□<br>Voltage Code ◄——<br>L: Lead Free<br>G: Halogen Free<br>Pin Code<br>1    2 |

■ **PIN CONFIGURATION**



V_CC
3

1          2
GND      $\overline{RESET}$

■ **PIN DESCRIPTION**

| No. | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | $\overline{RESET}$ | This pin will fall low after the $V_{CC}$'s falling below the reset threshold voltage and it also can remain asserted for at least 140ms min after $V_{CC}$'s rising upon the reset threshold. |
| 3 | $V_{CC}$ | Input of power supply. |

■ **BLOCK DIAGRAM**
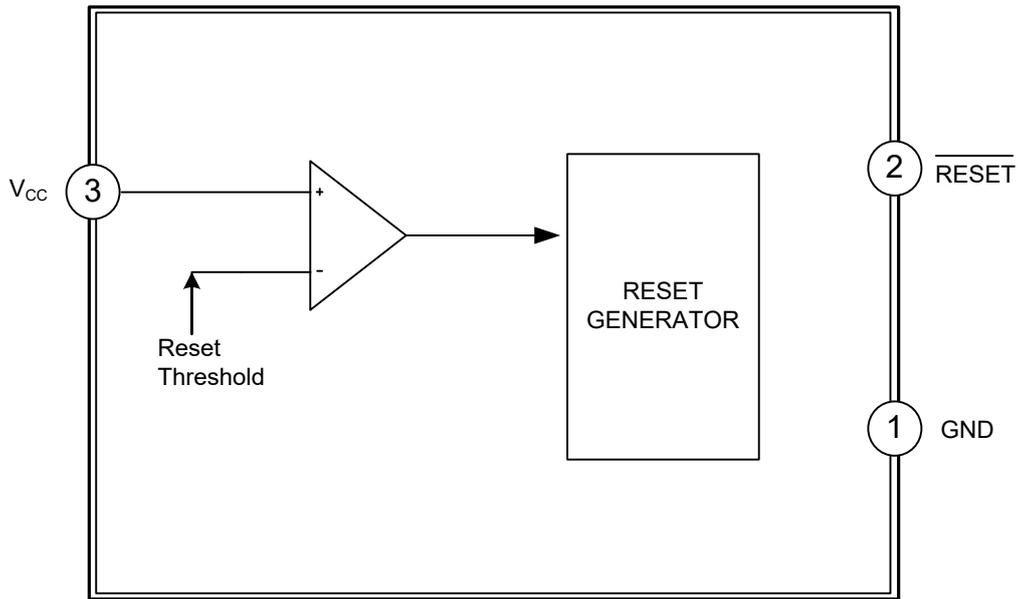


■ **FUNCTIONAL DIAGRAM**
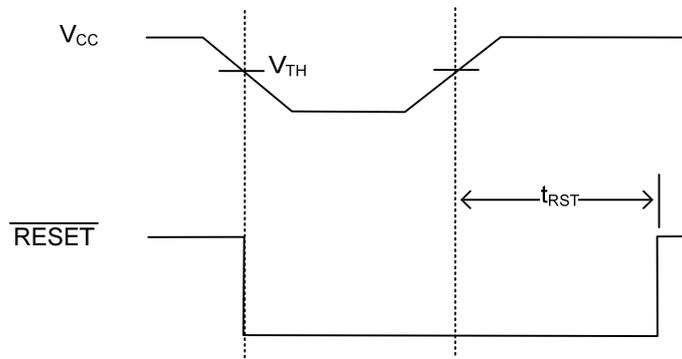


Reset Timing Diagram

■ **ABSOLUTE MAXIMUM RATING**

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Input Voltage | $V_{CC}$ | -0.3 ~ +6.0 | V |
| Input Current ($V_{CC}$) | $I_{IN}$ | 20 | mA |
| Output Current ($\overline{RESET}$) | $I_{OUT}$ | 20 | mA |
| Rate of Rise | $V_{CC(RR)}$ | 100 | V/μs |
| Power Dissipation ($T_A$ =+70°C) | $P_D$ | 300 | mW |
| Operating Temperature | $T_{OPR}$ | -40 ~ +125 | °C |
| Storage Temperature | $T_{STG}$ | -65 ~ +150 | °C |

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The device is not guaranteed to function outside its operating rating.

3. It is guarantee by design, not 100% be tested.

■ **ELECTRICAL CHARACTERISTICS**

**UIC809-B (2.93V)** ($V_{CC}$ =3.3V, $T_A$= 25°C, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Operating Voltage Range | $V_{CC}$ | $T_A$ =-40~+85°C | 1 | | 6 | V |
| Supply Current | $I_{CC}$ | $V_{CC}$=3.3V, no load | | 5 | 10 | μA |
| Reset Voltage Threshold | $V_{TH}$ | | 2.85 | 2.93 | 3.00 | V |
| Reset Timeout Period | $t_{RST}$ | | 140 | 240 | 560 | ms |
| $\overline{Reset}$ Output Voltage | $V_{OH}$ | $I_{SOURCE}$ =500μA | 2.64 | | | V |
| | $V_{OL}$ | $V_{CC}$ = $V_{TH}$ min, $I_{SINK}$ =1.2mA | | | 0.3 | V |
| | | $V_{CC}$>1V, $I_{SINK}$ =50μA, $T_A$=-40~+85°C | | | 0.3 | V |

Note: Production testing done at $T_A$ = +25°C, overtemperature limits ensured by QC screen.

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■ **TYPICAL APPLICATION CIRCUIT**
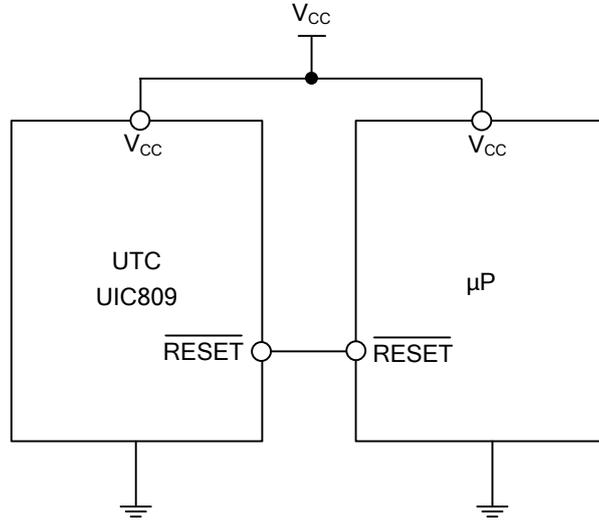
■ **APPLICATION INFORMATION**

**Microprocessor Reset**

As soon as $V_{CC}$ falls below the reset threshold voltage, the $\overline{\text{RESET}}$ pin is asserted. But the $\overline{\text{RESET}}$ pin can keep asserted for a period of 140ms after $V_{CC}$ rose above the reset threshold voltage. After a power failure the reset operation can keep the processor being reset and powers up properly.
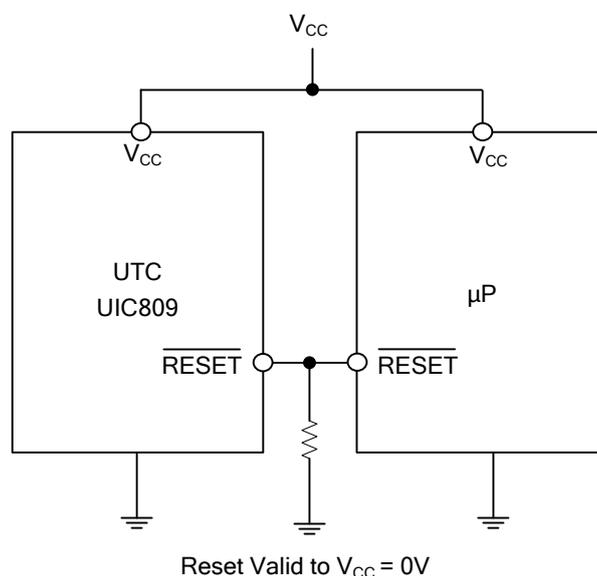
**V$_{CC}$ Transients**

The UTC **UIC809** series won't cause a reset typically as this situation: a negative-going transient 125mV below the reset threshold with a duration of 20μs or less.
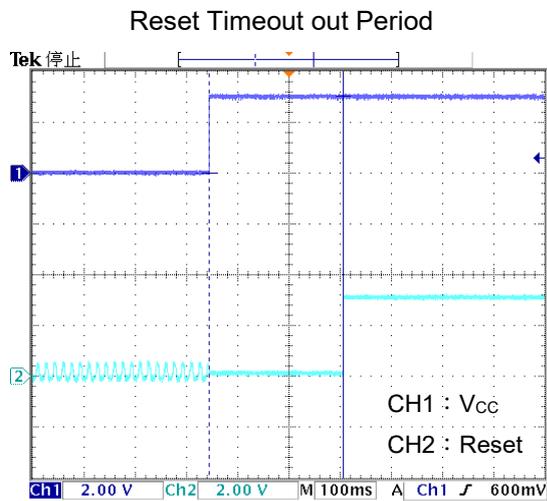
**Interfacing to Bidirectional Reset Pins**

Connecting a 4.7kΩ resistor in series with the UTC **UIC809** series output and the μP reset pin can make the UTC **UIC809** series interface with μPs with bidirectional reset pins.

**$\overline{\text{RESET}}$ Valid at Low Voltage**

As the figure below, adding a resistor which is recommended 100kΩ can ensure the $\overline{\text{RESET}}$ output remains low with $V_{CC}$ down to 0V. The size of the resistor should be not too large which will load the output excessively and not too small which can pull-down any stray leakage currents.



Reset Valid to $V_{CC}$ = 0V

■ **TYPICAL CHARACTERISTICS**

Reset Timeout out Period



CH1：V_CC
CH2：Reset

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