



US2236090D

Preliminary

LINEAR INTEGRATED CIRCUIT

ULTRA-SMALL, LOW-INPUT-VOLTAGE LOW R_{ON} LOAD SWITCH

DESCRIPTION

The UTC **US2236090D** is ultra-small, low R_{ON} single channel load switches with controlled turn on. The device contains a P-channel MOSFET that can operate over an input voltage range of 1.1 V to 3.6 V. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. In UTC **US2236090D** a 85- Ω on-chip load resistor is added for output quick discharge when switch is turned off.

FEATURES

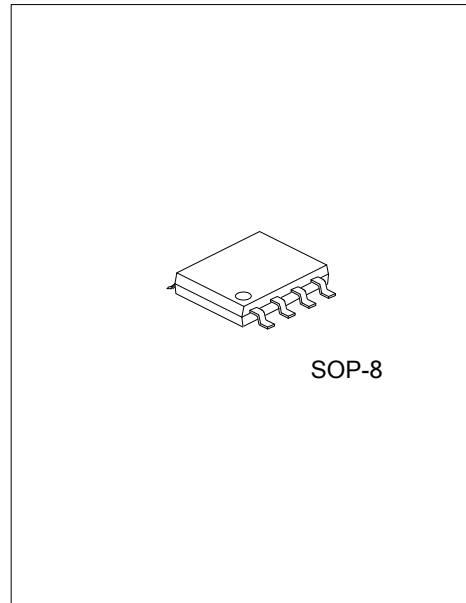
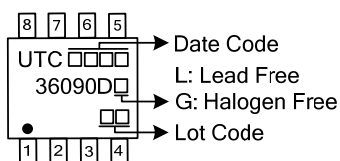
- * Input Voltage: 1.1V~3.6V
- * Ultra-Low ON-State Resistance
 - $R_{ON} = 66\text{ m}\Omega$ at $V_{IN} = 3.6\text{V}$
 - $R_{ON} = 75\text{ m}\Omega$ at $V_{IN} = 2.5\text{V}$
 - $R_{ON} = 90\text{ m}\Omega$ at $V_{IN} = 1.8\text{V}$
 - $R_{ON} = 135\text{ m}\Omega$ at $V_{IN} = 1.2\text{V}$
- * 500mA Maximum Continuous Switch Current
- * Quiescent Current $< 1\mu\text{A}$
- * Shutdown Current $< 1\mu\text{A}$
- * Low Control Input Threshold Enables Use of 1.2-V/1.8-V/2.5-V/3.3-V Logic
- * Controlled Slew Rate (5 μs Max at 3.6V)
- * Quick Output Discharge

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
US2236090DL-S08-R	US2236090DG-S08-R	SOP-8	Tape Reel

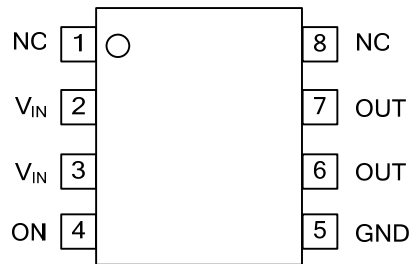
<p>US2236090DG-S08-R</p>	<p>(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



SOP-8

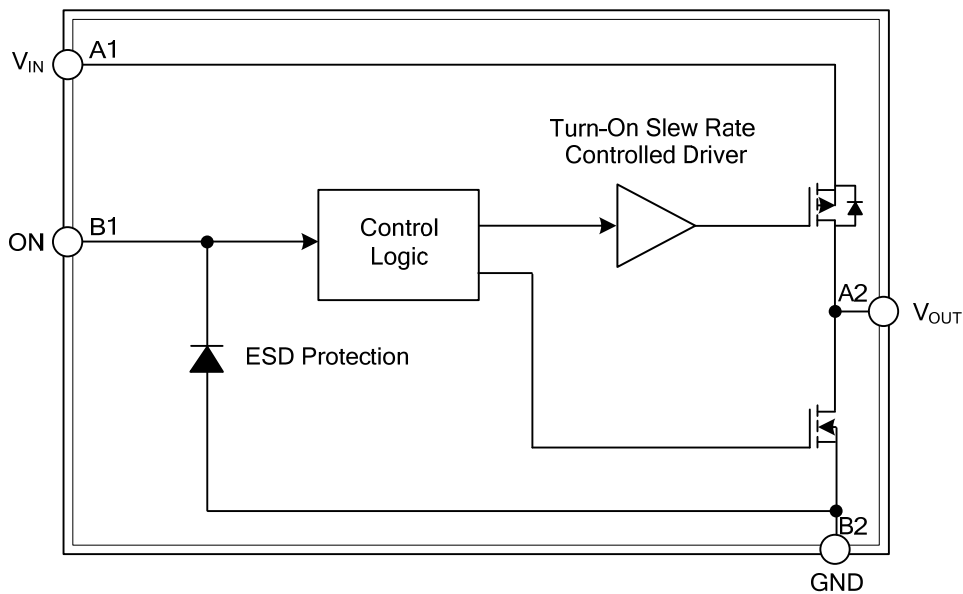
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1, 8	NC	
2, 3	V _{IN}	Switch input, bypass this input with a ceramic capacitor to ground
4	ON	Switch control input, active high
5	GND	Ground
6, 7	V _{OUT}	Switch output

■ BLOCK DIAGRAM



FUNCTION TABLE

ON (CONTROL INPUT)	V _{IN} to V _{OUT}	V _{OUT} TO GND
L	OFF	ON
H	ON	OFF

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage Range	V_{IN}	4	V
Output Voltage Range	V_{OUT}	$V_{IN} + 0.3$	V
Input Voltage Range	V_{ON}	4	V
Maximum Continuous Switch Current	I_{MAX}	0.5	A
Power Dissipation at $T_A=25^\circ\text{C}$	P_D	0.48	W
Maximum junction Temperature	T_J	+125	$^\circ\text{C}$
Operating Temperature Range	T_{OPR}	-40 ~ +85	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-65 ~ +150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	205	$^\circ\text{C/W}$

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}	1.1		3.6	V
Output Voltage Range	V_{OUT}			V_{IN}	V
High-Level Input Voltage, ON	V_{IH}	0.85		3.6	V
Low-Level Input Voltage, ON	V_{IL}			0.4	V
Input Capacitor	C_{IN}	1.0			μF

■ ELECTRICAL CHARACTERISTICS ($V_{IN}=1.1\text{V}\sim 3.6\text{V}$, $T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
Quiescent Current	I_{IN}	$I_{OUT}=0$, $V_{IN}=V_{ON}$			1	μA
OFF-State Supply Current	$I_{IN(OFF)}$	$V_{ON}=\text{GND}$, $\text{OUT}=\text{Open}$			1	μA
OFF-State Switch Current	$I_{IN(LEAKAGE)}$	$V_{ON}=\text{GND}$, $V_{OUT}=0$			1	μA
ON-State Resistance	R_{ON}	$I_{OUT}=-200\text{mA}$	$V_{IN}=3.6\text{V}$	66	90	$\text{m}\Omega$
			$V_{IN}=2.5\text{V}$	75	95	$\text{m}\Omega$
			$V_{IN}=1.8\text{V}$	90	115	$\text{m}\Omega$
			$V_{IN}=1.2\text{V}$	135	175	$\text{m}\Omega$
			$V_{IN}=1.1\text{V}$	157	275	$\text{m}\Omega$
Output Pulldown Resistance	r_{PD}	$V_{IN}=3.3\text{V}$, $V_{ON}=0$, $I_{OUT}=30\text{mA}$		85	135	Ω
ON-State Input Leakage Current	I_{ON}	$V_{ON}=1.1\text{V}\sim 3.6\text{V}$ or GND			1	μA

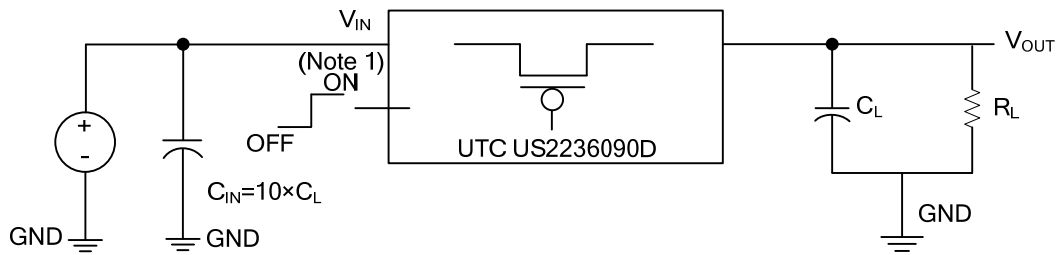
Note: Typical values are at $V_{IN}=3.3\text{V}$ and $T_A=25^\circ\text{C}$.

■ SWITCHING CHARACTERISTICS ($V_{IN}=3.6\text{V}$, $T_A=-40^\circ\text{C}\sim 85^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
Turn-ON Time	t_{ON}	$I_{OUT}=100\text{mA}$, $C_L=0.1\mu\text{F}$		1.2		μs
Turn-OFF Time	t_{OFF}	$I_{OUT}=100\text{mA}$, $C_L=0.1\mu\text{F}$		12	21	μs
V_{OUT} Rise Time	t_r	$I_{OUT}=100\text{mA}$, $C_L=0.1\mu\text{F}$		2.0		μs
V_{OUT} Fall Time	t_f	$I_{OUT}=100\text{mA}$, $C_L=0.1\mu\text{F}$		17	28	μs

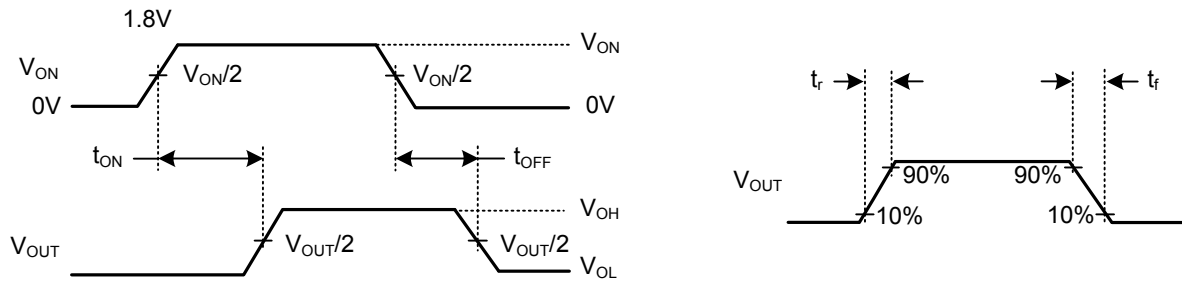
Note: Typical values are at $T_A=25^\circ\text{C}$.

■ TEST CIRCUIT AND WAVEFORMS



Note 1. t_{rise} and t_{fall} of the control signal is 100 ns.

TEST CIRCUIT



t_{ON}/t_{OFF} Waveforms

■ APPLICATION INFORMATION**ON/OFF Control**

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state as there is no fault. ON is active-high and has a low threshold, making it capable of interfacing with low voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2V, 1.8V, 2.5V or 3.3V GPIOs.

Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1.0 μ F ceramic capacitor, C_{IN} , placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor, this in order to avoid excessive voltage drop.

Output Capacitor (Optional)

Due to the integral body diode in the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} .

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for V_{IN} , V_{OUT} , and GND helps minimize the parasitic electrical effects along with minimizing the case-to-ambient thermal impedance.

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