



## US5C3305

Preliminary

CMOS IC

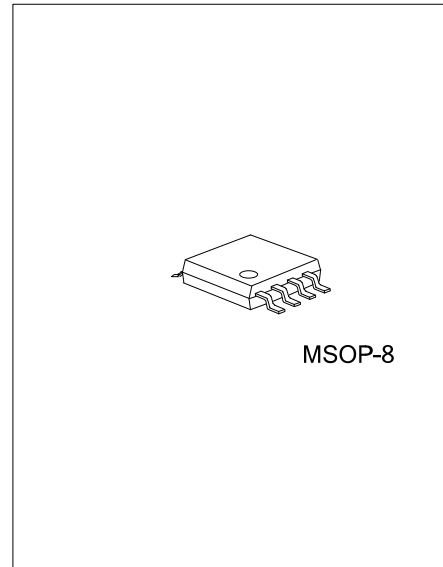
### 2-BIT BUS SWITCH WITH INDIVIDUAL ENABLES

#### DESCRIPTION

The UTC **US5C3305** consist of two independent 5Ω switches with fast individual enables. The “A” pin is connected to the “B” pin directly when the associated Bus Enable (BE) pin is set to “High”. The bus switch introduces no additional propagation delay or additional ground bounce noise.

#### FEATURES

- \* Low on-resistor between two ports (5Ω typical)
- \* Near-Zero propagation delay
- \* Direct bus connection when switches are ON
- \* Ultra Low Quiescent Power (0.2μA typical)
  - Ideally suited for notebook applications

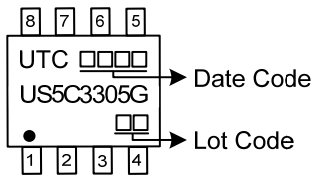


#### ORDERING INFORMATION

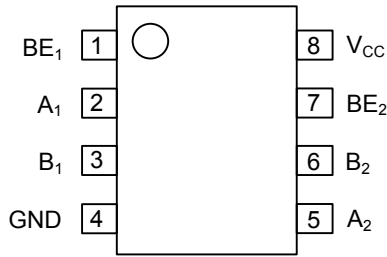
| Ordering Number | Package | Packing   |
|-----------------|---------|-----------|
| US5C3305G-SM1-R | MSOP-8  | Tape Reel |

|   |  |
|---|--|
| <p>US5C3305G-SM1-R</p> <ul style="list-style-type: none"> <li>(1)Packing Type</li> <li>(2)Package Type</li> <li>(3)Green Package</li> </ul> | <ul style="list-style-type: none"> <li>(1) R: Tape Reel</li> <li>(2) SM1: MSOP-8</li> <li>(3) G: Halogen Free and Lead Free</li> </ul> |
|---|--|

#### MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

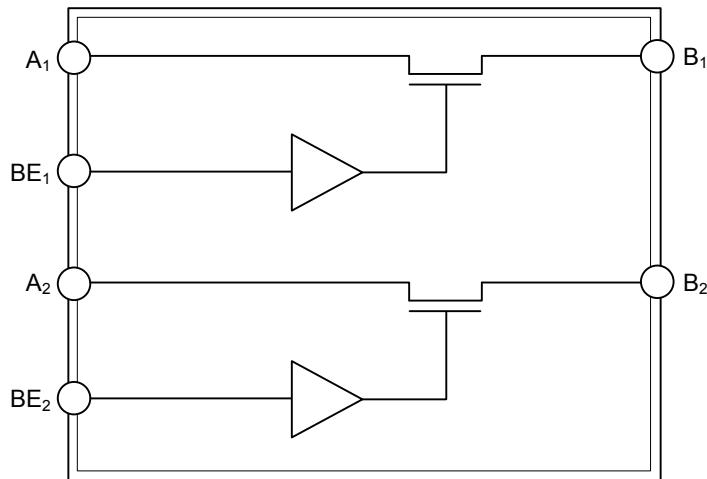
| PIN NO. | PIN NAME                        | DESCRIPTION   |
|---------|---------------------------------|---------------|
| 1, 7    | BE <sub>n</sub>                 | Switch Enable |
| 2, 5    | A <sub>1</sub> , A <sub>2</sub> | Bus A         |
| 3, 6    | B <sub>1</sub> , B <sub>2</sub> | Bus B         |
| 4       | GND                             | Ground        |
| 8       | V <sub>CC</sub>                 | Power         |

■ TRUTH TABLE (Note 1)

| BE <sub>n</sub> | A <sub>n</sub> | B <sub>n</sub> | V <sub>CC</sub> | Function   |
|-----------------|----------------|----------------|-----------------|------------|
| X (Note 2)      | Hi-Z           | Hi-Z           | GND             | Disconnect |
| L               | Hi-Z           | Hi-Z           | V <sub>CC</sub> | Disconnect |
| H               | B <sub>n</sub> | A <sub>n</sub> | V <sub>CC</sub> | Connect    |

Notes: 1. H=High Voltage Level, L=Low Voltage Level, Hi-Z=High Impedance, X=Don't Care  
 2. A pull-up resistor should be provided for power-up protection.

■ BLOCK DIAGRAM



### ■ ABSOLUTE MAXIMUM RATING ( $T_A=25^{\circ}\text{C}$ , unless otherwise specified)

(Above which the useful life may be impaired. For user guidelines, not tested.)

| PARAMETER                              | SYMBOL    | RATINGS   | UNIT               |
|--|-----------|-----------|--------------------|
| Supply Voltage to Ground Potential     |           | -0.5~+7.0 | V                  |
| DC Input Voltage                       |           | -0.5~+7.0 | V                  |
| DC Output Current                      |           | 120       | mA                 |
| Power Dissipation                      | $P_D$     | 0.35      | W                  |
| Storage Temperature                    | $T_{STG}$ | -65~+150  | $^{\circ}\text{C}$ |
| Ambient Temperature with Power Applied | $T_A$     | -40~+85   | $^{\circ}\text{C}$ |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

### ■ DC ELECTRICAL CHARACTERISTICS

(Over the Operating Range,  $T_A=-40^{\circ}\text{C}\sim+85^{\circ}\text{C}$ ,  $V_{CC}=4\text{V}\sim5.5\text{V}$ )

| PARAMETER                        | SYMBOL   | TEST CONDITIONS (Note 1)   | MIN  | TYP<br>(Note 2) | MAX     | UNIT          |
|----------------------------------|----------|--|------|-----------------|---------|---------------|
| Input HIGH Voltage               | $V_{IH}$ | Guaranteed Logic HIGH Level  |      | 2.0             |         | V             |
| Input LOW Voltage                | $V_{IL}$ | Guaranteed Logic LOW Level   | -0.5 |                 | 0.8     | V             |
| Input HIGH Current               | $I_{IH}$ | $V_{CC}=\text{Max.}$ , $V_{IN}=V_{CC}$   |      |                 | $\pm 1$ | $\mu\text{A}$ |
| Input LOW Current                | $I_{IL}$ | $V_{CC}=\text{Max.}$ , $V_{IN}=\text{GND}$   |      |                 | $\pm 1$ | $\mu\text{A}$ |
| High Impedance Output Current    | $I_{OZ}$ | $0\leq A$ , $B\leq V_{CC}$   |      |                 | $\pm 1$ | $\mu\text{A}$ |
| Low Impedance Output Current     | $I_{ON}$ | $0\leq A$ , $B\leq V_{CC}$   |      |                 | $\pm 1$ | $\mu\text{A}$ |
| Input Hysteresis at Control Pins | $V_H$    |  |      | 250             |         | mV            |
| Switch On-Resistance (Note 3)    | $R_{ON}$ | $V_{CC}=4.5\text{V}$ , $V_{IN}=0.0\text{V}$ ,<br>$I_{ON}=30\text{mA}$ or $64\text{mA}$ |      | 4               | 7       | $\Omega$      |
|                                  |          | $V_{CC}=4.5\text{V}$ , $V_{IN}=2.4\text{V}$ ,<br>$I_{ON}=-15\text{mA}$                 |      | 8               | 15      | $\Omega$      |

Notes: 1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type

2. Typical values are at  $V_{CC}=5.0\text{V}$ ,  $T_A=25^{\circ}\text{C}$  ambient and maximum loading.

3. Measured by the voltage drop between A and B pin at indicated current through the switch. On-Resistance is determined by the lower of the voltages on the two (A, B) pin

### ■ POWER SUPPLY CHARACTERISTICS

| PARAMETER                           | SYMBOL          | TEST CONDITIONS (Note 1)                              | MIN | TYP<br>(Note 2) | MAX | UNIT          |
|-------------------------------------|-----------------|---|-----|-----------------|-----|---------------|
| Quiescent Power Supply Current      | $I_{CC}$        | $V_{IN}=\text{GND}$ or $V_{CC}$                       |     | 0.1             | 3.0 | $\mu\text{A}$ |
| Supply Current per Input @ TTL HIGH | $\Delta I_{CC}$ | $V_{CC}=\text{Max.}$<br>$V_{IN}=3.4\text{V}$ (Note 3) |     |                 | 2.5 | mA            |

Notes: 1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.

2. Typical values are at  $V_{CC}=5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.

3. Per TTL driven input ( $V_{IN}=3.4\text{V}$ , control inputs only); A and B pins do not contribute to  $I_{CC}$ .

### ■ CAPACITANCE ( $T_A=25^{\circ}\text{C}$ , $f=1\text{MHz}$ )

| PARAMETER (Note 1)          | SYMBOL    | TEST CONDITIONS (Note 1) | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------|--------------------------|-----|-----|-----|------|
| Input Capacitance           | $C_{IN}$  | $V_{IN}=0\text{V}$       |     | 3   |     | pF   |
| A/B Capacitance, Switch Off | $C_{OFF}$ |                          |     | 5   |     | pF   |
| A/B Capacitance, Switch On  | $C_{ON}$  |                          |     | 10  |     | pF   |

Note: This parameter is determined by device characterization but is not production tested.

■ SWITCHING CHARACTERISTICS OVER OPERATING RANGE ( $C_L=50\text{pF}$ ,  $R_L=500\Omega$ )

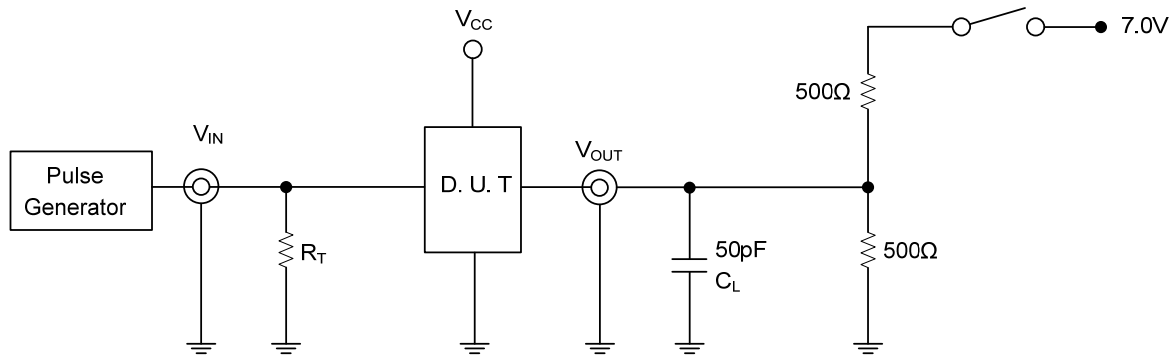
| PARAMETER   | SYMBOL            | TEST CONDITIONS<br>(Note 1) | MIN | TYP | MAX  | UNIT |
|---|-------------------|-----------------------------|-----|-----|------|------|
| Propagation Delay Time Signal A to B,<br>B to A (Note 2, 3) | $t_{PLH}/t_{PHL}$ | $V_{CC}=4\text{V}$          |     |     | 0.25 | ns   |
|   |                   | $V_{CC}=5\text{V}\pm 10\%$  | 1.0 |     | 0.25 | ns   |
| Bus Enable Time   | $t_{PZH}/t_{PZL}$ | $V_{CC}=4\text{V}$          |     |     | 5.5  | ns   |
|   |                   | $V_{CC}=5\text{V}\pm 10\%$  | 1.0 |     | 4.9  | ns   |
| Bus Disable Time  | $t_{PHZ}/t_{PLZ}$ | $V_{CC}=4\text{V}$          |     |     | 4.5  | ns   |
|   |                   | $V_{CC}=5\text{V}\pm 10\%$  |     |     | 4.2  | ns   |

Notes: 1. See test circuit and waveforms.

2. This parameter is guaranteed but not tested on Propagation Delays.

3. The bus switch contributes no propagational delay other than the RC delay of the On-Resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 50pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

■ TEST CIRCUIT



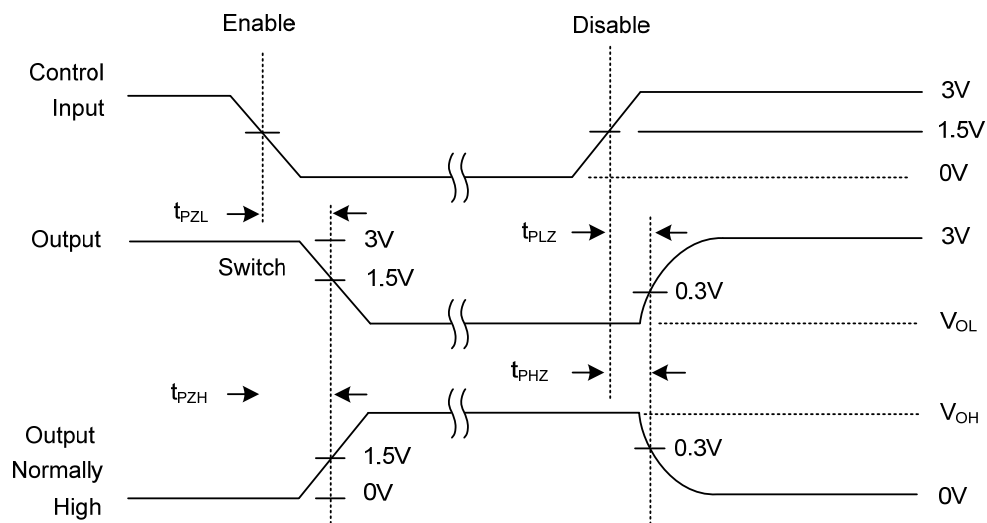
■ SWITCH POSITIONS

| Test             | Switch |
|------------------|--------|
| Open Drain       |        |
| Disable LOW      | 7V     |
| Enable LOW       |        |
| All Other Inputs | Open   |

Note:  $C_L$ =Load Capacitance: includes jig and probe capacitance.

$R_T$ =Termination Resistance: should be equal to the  $Z_{OUT}$  of the Pulse Generator.

■ ENABLE AND DISABLE TIMING



- Notes: 1. Input Control Enable = Low; Input Control Disable=High
- 2. Pulse Generator for All Pulses: Rate  $\leq 1.0$  MHz;  $Z_{OUT} \leq 50\Omega$ ;  $t_F, t_R, \leq 2.5$ ns.

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