



## UTRS485

CMOS IC

### FAIL-SAFE, 4.5MBPS, RS-485 / RS-422 TRANSCEIVERS WITH $\pm 12KV$ ESD-PROTECTED

#### DESCRIPTION

The UTC **UTRS485** is a half-duplex transceiver designed for RS-485 data bus network, which contains one transmitter and one receiver. The UTC **UTRS485** features a fail-safe receiver, which guarantees the receiver to output high when the receiver inputs are open.

The UTC **UTRS485** also features a hot-swap glitch free protection circuits which guarantee outputs of both the transmitter and the receiver in a high impedance state during the power up period. So that the large short current from power to ground will be disabled by glitch free function, which will save the power and enhance the efficiency of the power up.

The UTC **UTRS485** is optimized for signal rates up to 4.5Mbps with differential voltage of 2.3V. The UTC **UTRS485** also has the thermal shutdown function when the temperature is over 150°C and the protection of the current limitation in the transmitter to protect the itself from the damage by the system-fault conditions during normal operation.

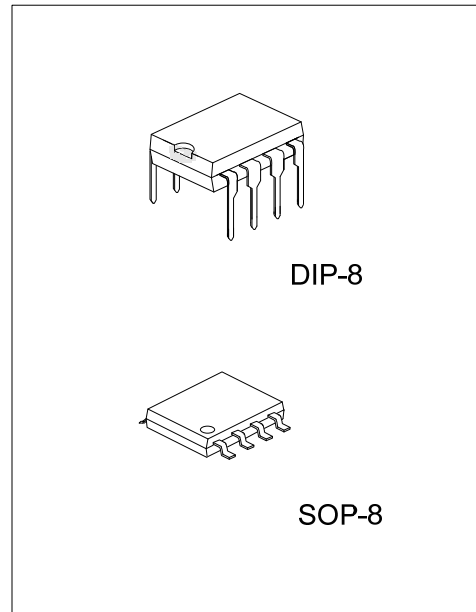
#### FEATURES

- \* Meet the requirements of the EIA/TIA-485 standards.
- \* 5.0V single power supply.
- \* True fail-safe receiver while maintaining EIA/TIA-485 compatibility.
- \* Hot-Swap glitch free protection on control inputs.
- \* Up to 32 transceivers on the bus.
- \* Driver short circuit current limit.
- \* Thermal shutdown for overload protection.

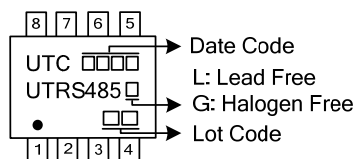
#### ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UTRS485L-D08-T	UTRS485G-D08-T	DIP-8	Tube
UTRS485L-S08-R	UTRS485G-S08-R	SOP-8	Tape Reel

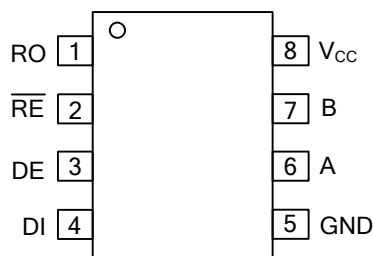
<p>UTRS485G-D08-T</p>	<p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) D08: DIP-8, S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



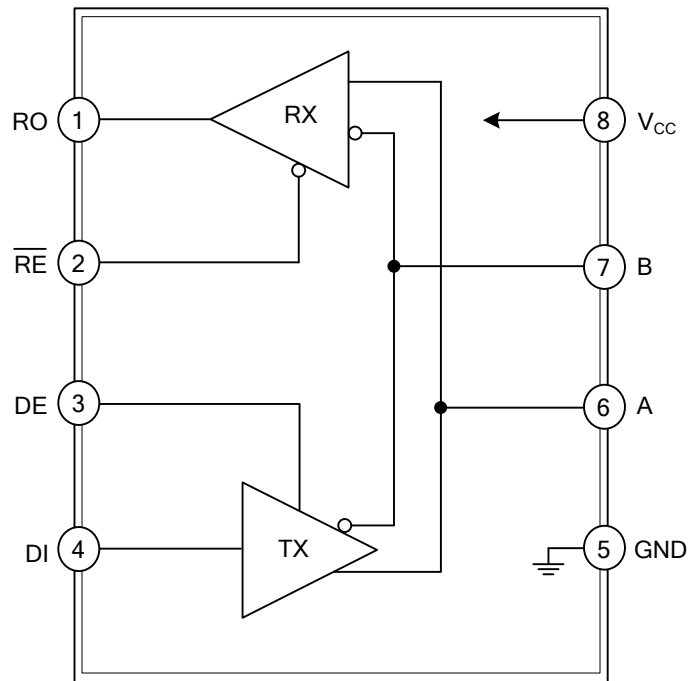
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	RO	Receiver output: if $A > B$ by 200mV, RO will be high; if $A < B$ by 200mV, RO will be low.
2	$\overline{RE}$	Receiver output enable. RO is enable when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	GND	Ground
6	A	Non-inverting receiver input and non-inverting driver output
7	B	Inverting receiver input and inverting driver output
8	$V_{CC}$	Positive supply; $4.75V \leq V_{CC} \leq 5.25V$

■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	7.0	V
Control Input Voltage ( $\overline{RE}$ , DE)		$V_{CC}$	V
Driver Input Voltage (DI)	DI	$V_{CC}$	V
Driver Output Voltage (A, B)		$\pm 12.5$	V
Receiver Input Voltage (A, B)		$\pm 12.5$	V
Receiver Output Voltage (RO)		$V_{CC}$	V
Continuous Power Dissipation ( $T_A=+70^\circ\text{C}$ )	DIP-8	800	mW
	SOP-8	625	mW
Operating Temperature Ranges	$T_{OPR}$	-40 ~ +85	$^\circ\text{C}$
Storage Temperature Range	$T_{STG}$	-65 ~ +160	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ DC ELECTRICAL CHARACTERISTICS

( $V_{CC}=5.0\text{V} \pm 5\%$ ,  $T_A=T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. (Note 1, 2))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Differential Driver Output (No Load)	$V_{OD1}$				5.0	V
Differential Driver Output (with Load)	$V_{OD2}$	R=50 $\Omega$ (RS-422)	2.0			V
		Fig.1, R=27 $\Omega$ (RS-485)	1.5		5.0	V
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	$\Delta V_{OD}$	Fig.1, R=27 $\Omega$ or 50 $\Omega$			0.2	V
Driver Common-Mode Output Voltage	$V_{OC}$	Fig.1, R=27 $\Omega$ or 50 $\Omega$			3.0	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	$\Delta V_{OC}$	Fig.1, R=27 $\Omega$ or 50 $\Omega$			0.2	V
Input High Voltage	$V_{IH1}$	DE, DI, $\overline{RE}$	2.0			V
Input Low Voltage	$V_{IL1}$	DE, DI, $\overline{RE}$			0.8	V
Input Current	$I_{IN1}$	DE, DI, $\overline{RE}$			$\pm 2.0$	$\mu\text{A}$
Input Current (A, B)	$I_{IN2}$	DE=0V; $V_{CC}=0\text{V}$ or 5.25V	$V_{IN}=12\text{V}$		1.0	mA
			$V_{IN}=-7\text{V}$		-0.8	mA
Receiver Differential Threshold Voltage	$V_{TH}$	$V_{CM}=+2.5\text{V}$	-0.2		0.2	V
Receiver Input Hysteresis	$\Delta V_{TH}$	$V_{CM}=0\text{V}$		70		mV
Receiver Output High Voltage	$V_{OH}$	$I_O=-4\text{mA}$ , $V_{ID}=200\text{mV}$	3.5			V
Receiver Output Low Voltage	$V_{OL}$	$I_O=4\text{mA}$ , $V_{ID}=-200\text{mV}$			0.5	V
Three-State (High Impedance) Output Current at Receiver	$I_{OZR}$	$0.4\text{V} \leq V_O \leq 2.4\text{V}$			$\pm 1.0$	$\mu\text{A}$
Receiver Input Resistance	$R_{IN}$	$-7\text{V} \leq V_{CM} \leq +12\text{V}$	12			k $\Omega$
No-Load Supply Current (Note 3)	$I_{CC}$	$\overline{RE}=0\text{V}$ or $V_{CC}$	DE= $V_{CC}$	500	900	$\mu\text{A}$
			DE=0V	300	500	$\mu\text{A}$
Driver Short-Circuit Current, $V_O=High$	$I_{OSD1}$	$-7\text{V} \leq V_O \leq 12\text{V}$ (Note 4)	35		250	mA
Driver Short-Circuit Current, $V_O=Low$	$I_{OSD2}$	$-7\text{V} \leq V_O \leq 12\text{V}$ (Note 4)	35		250	mA
Receiver Short-Circuit Current	$I_{OSR}$	$0\text{V} \leq V_O \leq V_{CC}$	$\pm 7$		$\pm 95$	mA

## ■ SWITCHING CHARACTERISTICS

( $V_{CC}=+5.0V \pm 5\%$ ,  $T_A=T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.) (Note 1, 2)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Input to Output	$t_{DPLH}$	Fig.3 and 5, $R_{DIFF}=54\Omega$ , $C_{L1}=C_{L2}=100pF$		50	200	ns
	$t_{DPHL}$			50	200	ns
Driver Output Skew to Output	$t_{DSKEW}$	Fig.3 and 5, $R_{DIFF}=54\Omega$ , $C_{L1}=C_{L2}=100pF$		10		ns
Driver Rise or Fall Time	$t_{DR}$ , $t_{DF}$	Fig.3 and 5, $R_{DIFF}=54\Omega$ , $C_{L1}=C_{L2}=100pF$		15	150	ns
Driver Enable to Output High	$t_{DZH}$	Fig.4 and 6, $C_L=100pF$ , S2 Closed		80	200	ns
Driver Enable to Output Low	$t_{DZL}$	Fig.4 and 6, $C_L=100pF$ , S1 Closed		80	200	ns
Driver Disable Time from Low	$t_{DLZ}$	Fig.4 and 6, $C_L=15pF$ , S1 Closed		80	200	ns
Driver Disable Time from High	$t_{DHZ}$	Fig.4 and 6, $C_L=15pF$ , S2 Closed		80	200	ns
Receiver Input to Output	$t_{RPLH}$ , $t_{RPHL}$	Fig.3 and 7, $R_{DIFF}=54\Omega$ , $C_{L1}=C_{L2}=100pF$		500		ns
$ t_{PLH} - t_{PHL} $ Differential Receiver Skew	$t_{RSKD}$	Fig.3 and 7, $R_{DIFF}=54\Omega$ , $C_{L1}=C_{L2}=100pF$		100		ns
Receiver Enable to Output Low	$t_{RZL}$	Fig.2 and 8, $C_{RL}=15pF$ , S1 Closed		30	200	ns
Receiver Enable to Output High	$t_{RZH}$	Fig.2 and 8, $C_{RL}=15pF$ , S2 Closed		30	200	ns
Receiver Disable Time from Low	$t_{RLZ}$	Fig.2 and 8, $C_{RL}=15pF$ , S1 Closed		30	200	ns
Receiver Disable Time from High	$t_{RHZ}$	Fig.2 and 8, $C_{RL}=15pF$ , S2 Closed		30	200	ns
Maximum Data Rate	$f_{MAX}$				4.5	Mbps

Notes: 1. All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to device ground unless otherwise specified.

2. All typical specifications are given for  $V_{CC}=5.0V$  and  $T_A=+25^\circ C$

3. Supply current specification is valid for loaded transmitters when  $DE=0V$

4. Applies to peak current

■ FUNCTION TABLE

Table 1 TRANSMITTING

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z	High-Z

Table 2 RECEIVING

INPUTS			OUTPUTS
$\overline{RE}$	DE	A-B	RO
0	0	$\geq +0.2V$	1
0	0	$\leq -0.2V$	0
0	0	Inputs open	1
1	0	X	High-Z

X = Don't care

High-Z = High impedance

## TEST CIRCUIT

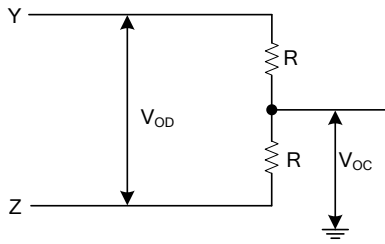


Fig. 1 Driver DC Test Load

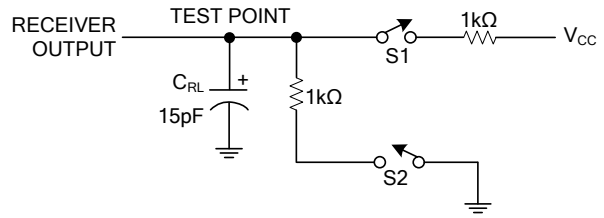


Fig. 2 Receiver Timing Test Load

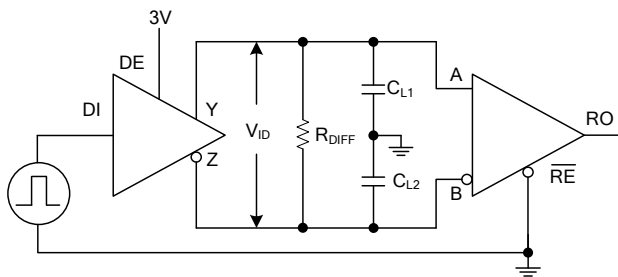


Fig. 3 Driver/Receiver Timing Test Circuit

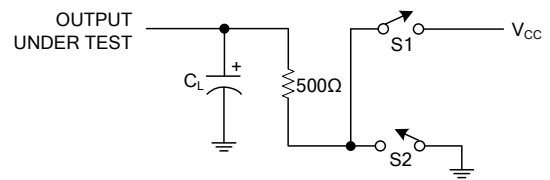


Fig. 4 Driver Timing Test Load

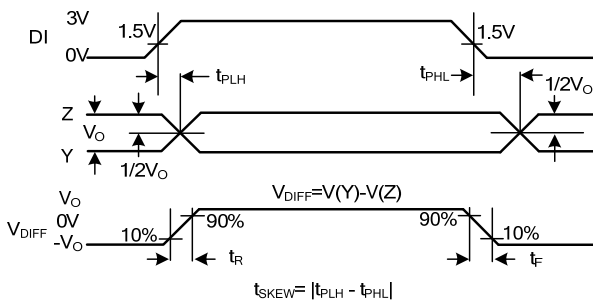


Fig. 5 Driver Propagation Delays

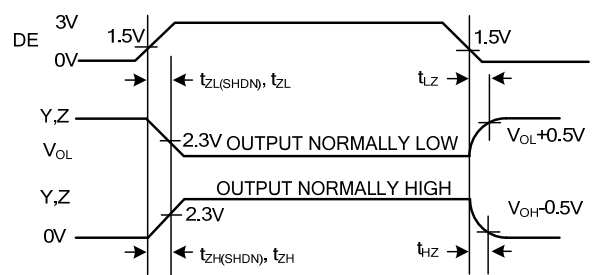


Fig. 6 Driver Enable and Disable Times

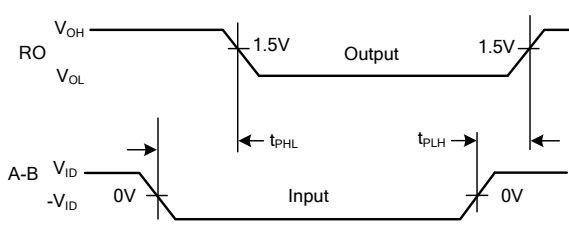


Fig. 7 Receiver Propagation Delays

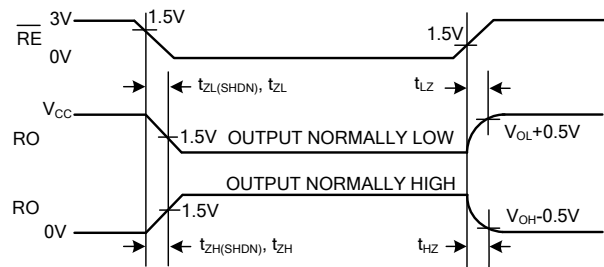
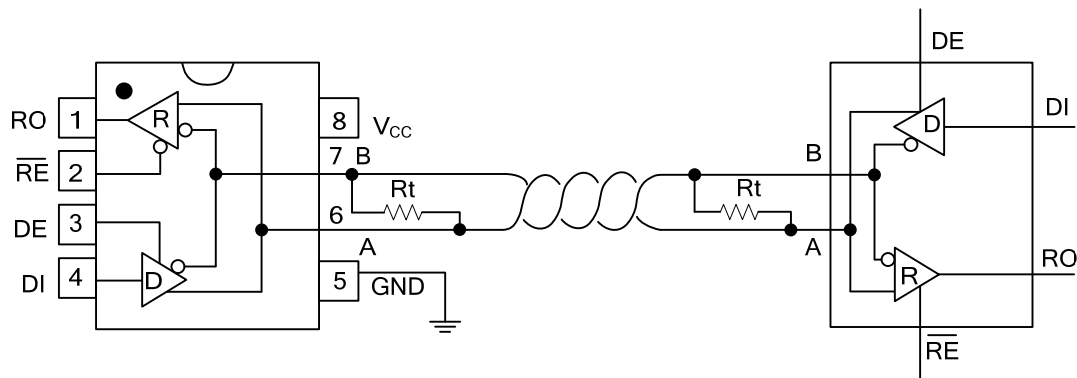


Fig. 8 Receiver Enable and Disable Times

■ TYPICAL APPLICATION CIRCUIT



Note: Pin labels Y and Z on timing, test, and waveform diagrams refer to pins A and B when DE is high.

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