



## UTT100N08M

### POWER MOSFET

## 100A, 80V N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET

### DESCRIPTION

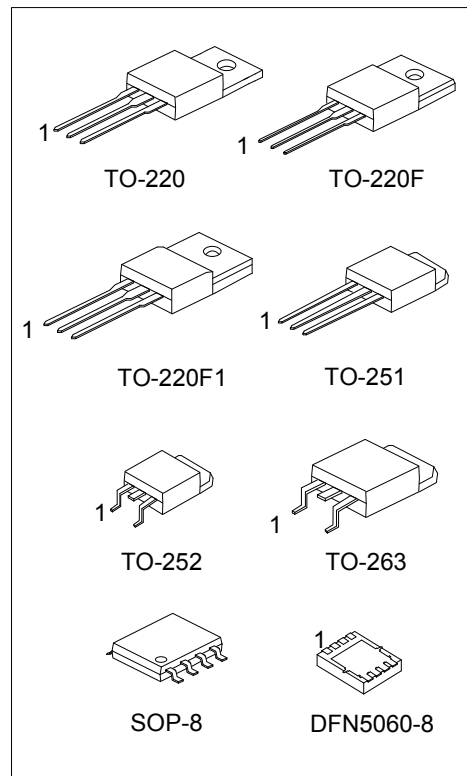
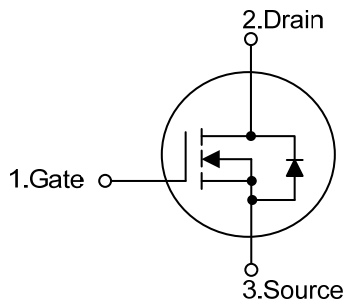
The UTC **UTT100N08M** is a N-channel Power MOSFET, it uses UTC's advanced technology that is uniquely optimized to provide an extremely low on-state resistance and low gate charge, etc.

The UTC **UTT100N08M** is suitable for synchronous rectification in SMPS, UPS, high speed power switching, etc.

### FEATURES

- \*  $R_{DS(ON)} \leq 12m\Omega @ V_{GS}=10V, I_D=40A$
- \*  $R_{DS(ON)} \leq 14m\Omega @ V_{GS}=4.5V, I_D=20A$
- \* High power and current handling capability
- \* High speed switching
- \* Low gate charge

### SYMBOL



### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UTT100N08ML-TA3-T	UTT100N08MG-TA3-T	TO-220	G	D	S	-	-	-	-	-	Tube
UTT100N08ML-TF1-T	UTT100N08MG-TF1-T	TO-220F1	G	D	S	-	-	-	-	-	Tube
UTT100N08ML-TF3-T	UTT100N08MG-TF3-T	TO-220F	G	D	S	-	-	-	-	-	Tube
UTT100N08ML-TM3-T	UTT100N08MG-TM3-T	TO-251	G	D	S	-	-	-	-	-	Tube
UTT100N08ML-TN3-R	UTT100N08MG-TN3-R	TO-252	G	D	S	-	-	-	-	-	Tape Reel
UTT100N08ML-TQ2-T	UTT100N08MG-TQ2-T	TO-263	G	D	S						Tube
UTT100N08ML-TQ2-R	UTT100N08MG-TQ2-R	TO-263	G	D	S						Tape Reel
UTT100N08ML-S08-R	UTT100N08MG-S08-R	SOP-8	S	S	S	G	D	D	D	D	Tape Reel
UTT100N08ML-K08-5060-R	UTT100N08MG-K08-5060-R	DFN5060-8	S	S	S	G	D	D	D	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UTT100N08MG-TA3-T</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) TA3: TO-220, TF1: TO-220F1, TF3: TO-220F, TM3: TO-251, TN3: TO-252, S08: SOP-8, K08-5060: DFN5060-8 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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### MARKING

Package	Marking
TO-220 TO-220F TO-220F1 TO-251 TO-252 TO-263	<p>UTC UTT 100N08M □□□□□□□□ Lot Code ← → Date Code L: Lead Free G: Halogen Free</p>
SOP-8	<p>8 7 6 5 UTT □□□□ 100N08M □ • □□ 1 2 3 4 Date Code L: Lead Free G: Halogen Free Lot Code</p>
DFN5060-8	<p>UTC UTT 100N08M • □□□□□□ Lot Code ← → Date Code</p>

■ ABSOLUTE MAXIMUM RATING ( $T_A=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	80	V
Gate-Source Voltage		$V_{GSS}$	$\pm 20$	V
Drain Current ( $T_C=25^{\circ}\text{C}$ ) (Note2)	Continuous	TO-220/TO-220F TO-220F1/TO-263	100	A
		TO-251/TO-252	80	A
		SOP-8	34	A
		DFN5060-8	50	A
		Pulsed Drain Current (Note 3)	$I_{DM}$	200
Avalanche Current		$I_{AS}$	50	A
Avalanche Energy (Note4)		$E_{AS}$	140.5	mJ
Power Dissipation ( $T_C=25^{\circ}\text{C}$ )		TO-220/TO-263	154	W
		TO-220F TO-220F1	35	W
		TO-251 TO-252	60	W
		SOP-8	7.5	W
		DFN5060-8	56	W
Junction Temperature		$T_J$	+150	$^{\circ}\text{C}$
Storage Temperature Range		$T_{STG}$	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Current limited by bond wire.

3. Repetitive Rating: Pulse width limited by maximum junction temperature.

4.  $L=0.1\text{mH}$ ,  $I_{AS}=53\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J = 25^{\circ}\text{C}$

5.  $I_{SD} \leq 20\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 150^{\circ}\text{C}$

■ THERMAL RESISTANCES CHARACTERISTICS

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	steady state	TO-220/TO-263 TO-220F TO-220F1	62.5	$^{\circ}\text{C}/\text{W}$
		TO-251 TO-252	110	$^{\circ}\text{C}/\text{W}$
		SOP-8	50 (Note)	$^{\circ}\text{C}/\text{W}$
		DFN5060-8	40.3 (Note)	$^{\circ}\text{C}/\text{W}$
		Junction to Case	steady state	TO-220/TO-263
TO-220F TO-220F1	3.57	$^{\circ}\text{C}/\text{W}$		
TO-251 TO-252	2.08 (Note)	$^{\circ}\text{C}/\text{W}$		
SOP-8	16.67 (Note)	$^{\circ}\text{C}/\text{W}$		
DFN5060-8	2.23 (Note)	$^{\circ}\text{C}/\text{W}$		

Note: The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.

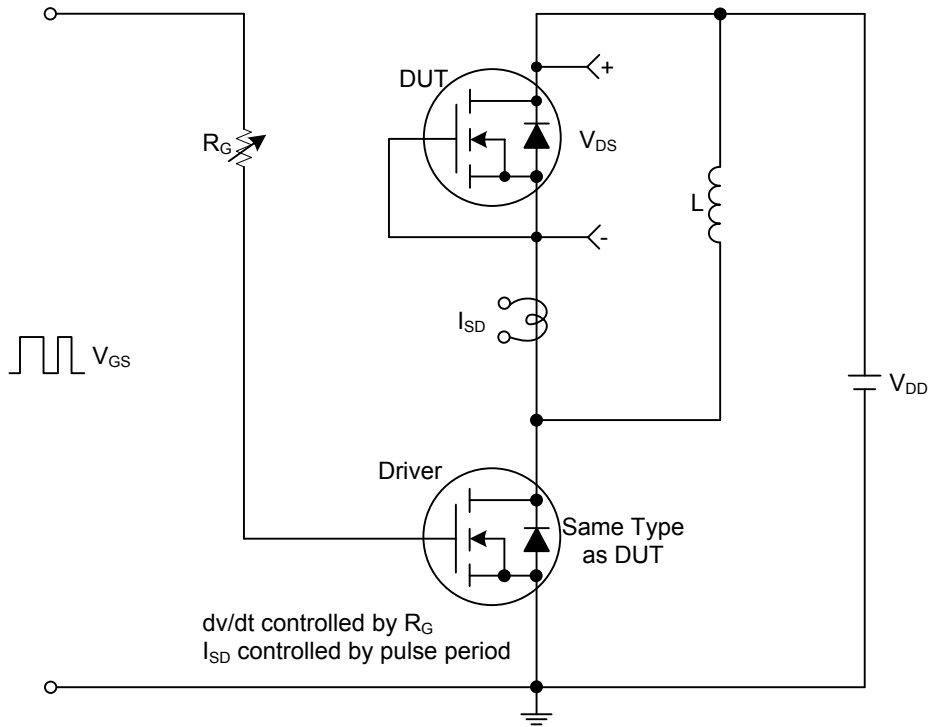
■ ELECTRICAL CHARACTERISTICS (T<sub>A</sub> =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	80			V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V			1	μA
Gate-Source Leakage Current	Forward	I <sub>GSS</sub> V <sub>GS</sub> =+20V, V <sub>DS</sub> =0V V <sub>GS</sub> =-20V, V <sub>DS</sub> =0V			+100	nA
	Reverse				-100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =40A			12	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A			14	mΩ
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1.0MHz		5503		pF
Output Capacitance	C <sub>OSS</sub>			356		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			172		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge (Note)	Q <sub>G</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> =10V, I <sub>D</sub> =100A I <sub>G</sub> =100μA (Note1,2)		81		nC
Gate to Source Charge	Q <sub>GS</sub>			23		nC
Gate to Drain Charge	Q <sub>GD</sub>			8		nC
Turn-on Delay Time (Note)	t <sub>D(ON)</sub>	V <sub>DD</sub> =40V, V <sub>GS</sub> =10V, I <sub>D</sub> =100A, R <sub>G</sub> =3.3Ω (Note1,2)		16		ns
Rise Time	t <sub>R</sub>			17.5		ns
Turn-off Delay Time	t <sub>D(OFF)</sub>			56		ns
Fall-Time	t <sub>F</sub>			21		ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	I <sub>S</sub>				100	A
Maximum Body-Diode Pulsed Current	I <sub>SM</sub>				200	A
Drain-Source Diode Forward Voltage (Note)	V <sub>SD</sub>	I <sub>F</sub> =100A, V <sub>GS</sub> =0V		0.85	1.4	V
Body Diode Reverse Recovery Time (Note)	t <sub>rr</sub>	I <sub>F</sub> =30A, dI <sub>S</sub> /dt=100A/μs		33		ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>				31	

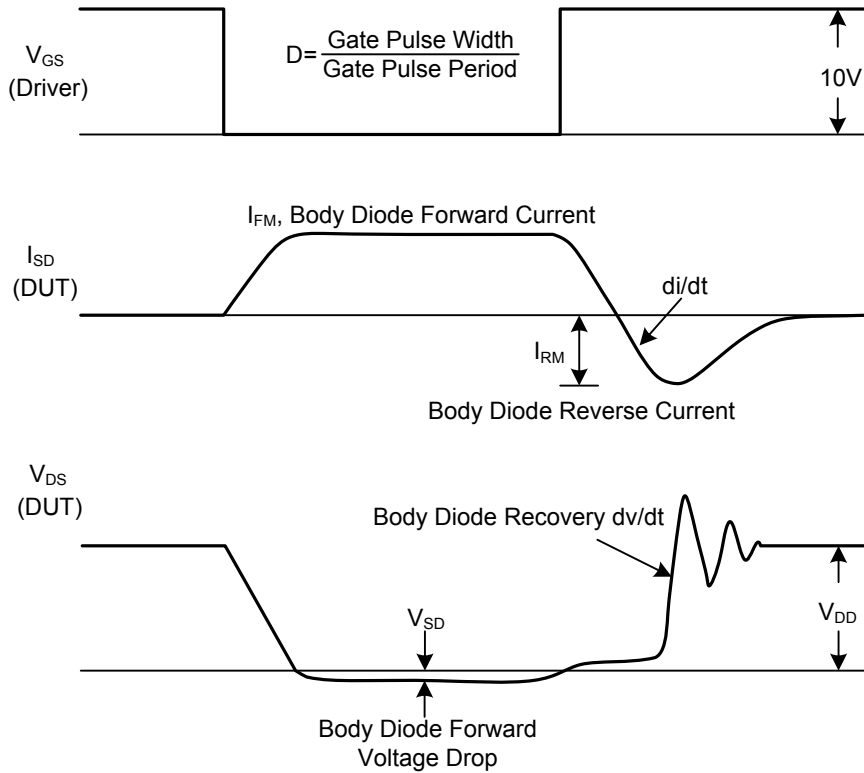
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

## TEST CIRCUITS AND WAVEFORMS



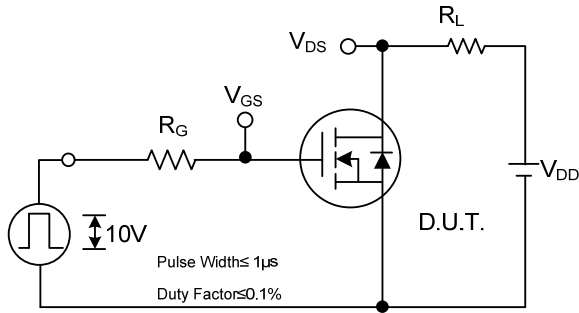
**Peak Diode Recovery dv/dt Test Circuit**



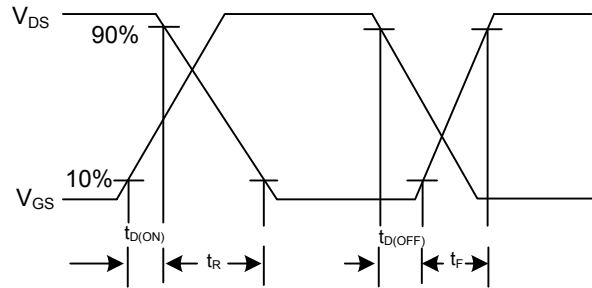
**Peak Diode Recovery dv/dt Test Circuit and Waveforms**

**Peak Diode Recovery dv/dt Waveforms**

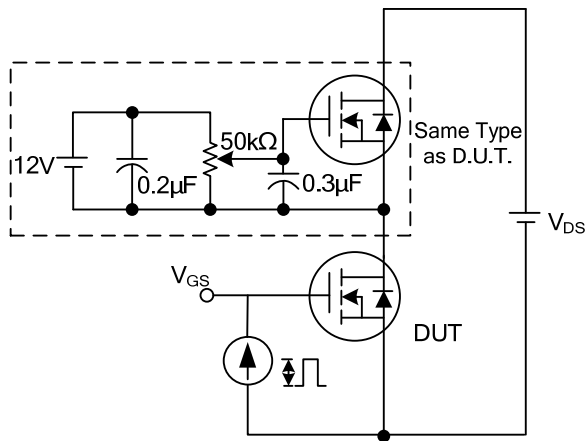
## TEST CIRCUITS AND WAVEFORMS



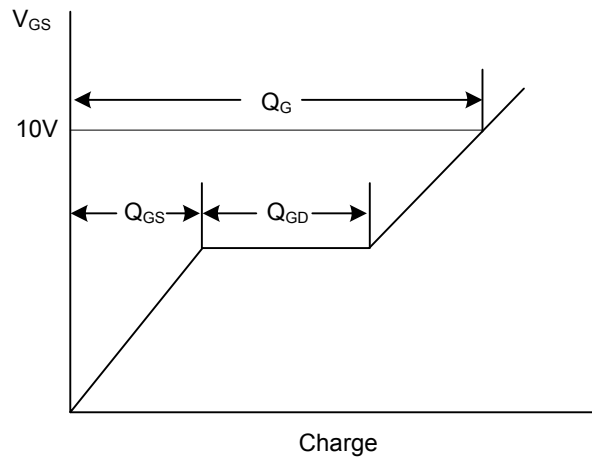
**Switching Test Circuit**



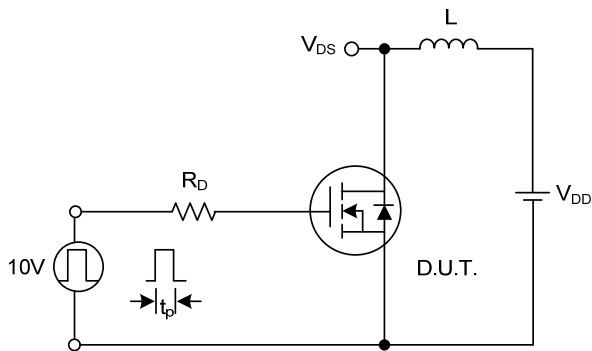
**Switching Waveforms**



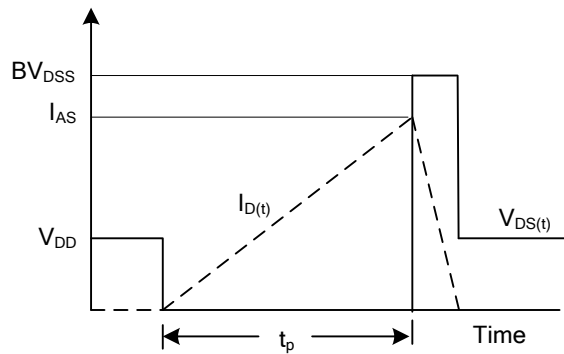
**Gate Charge Test Circuit**



**Gate Charge Waveform**

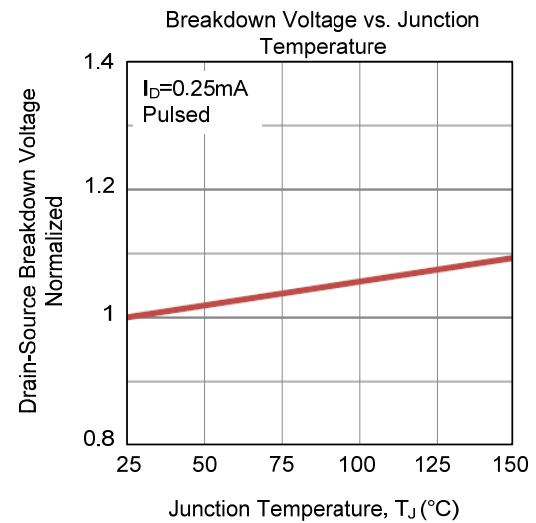
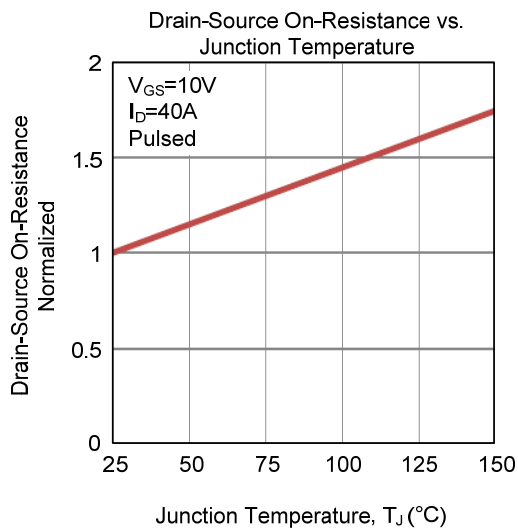
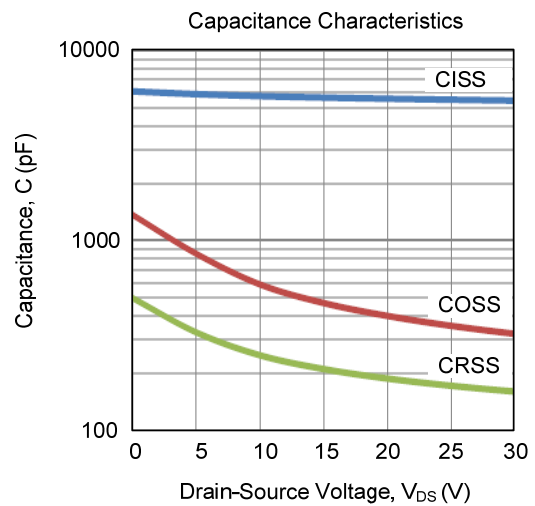
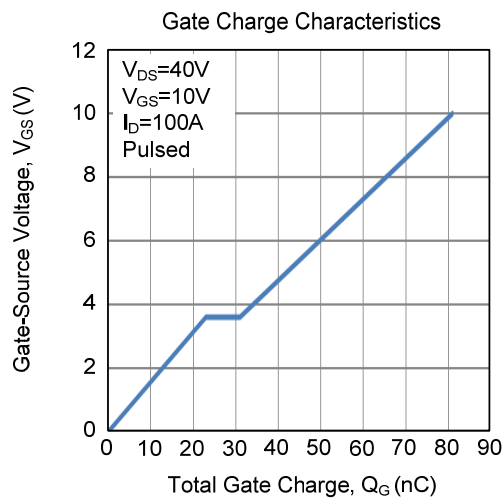
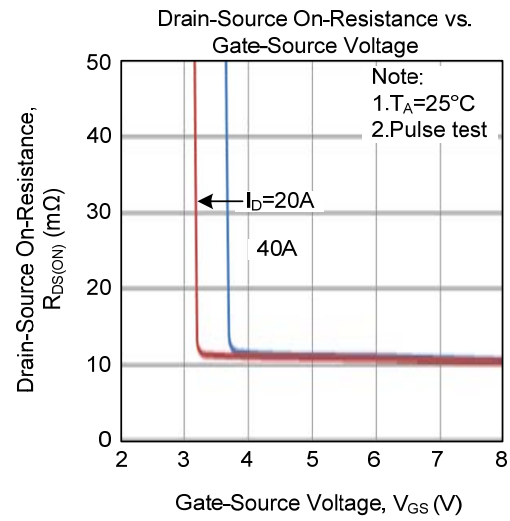
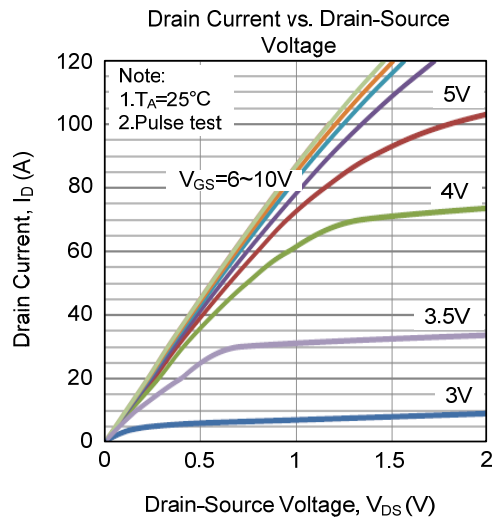


**Unclamped Inductive Switching Test Circuit**

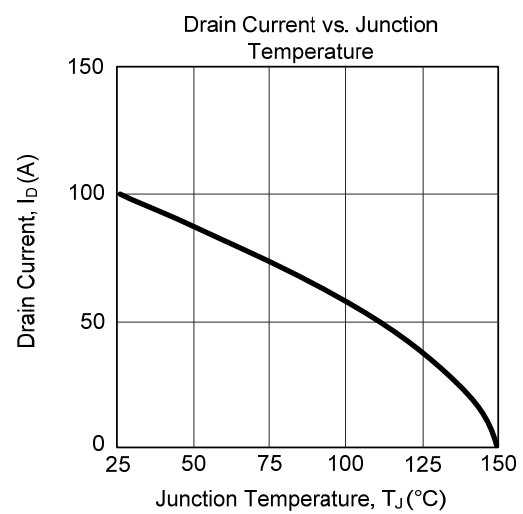
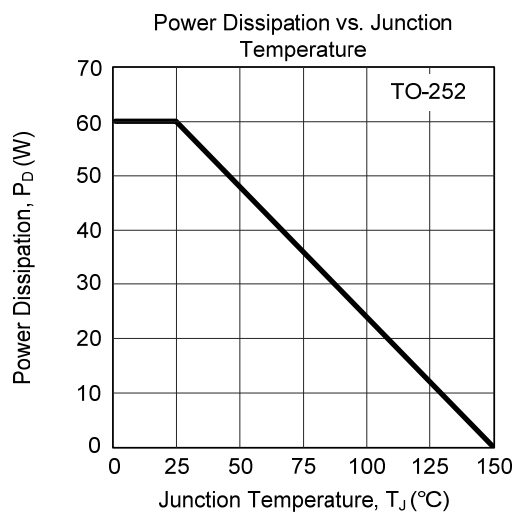
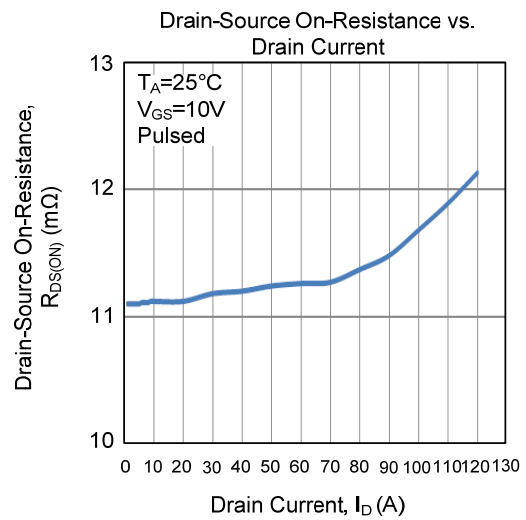
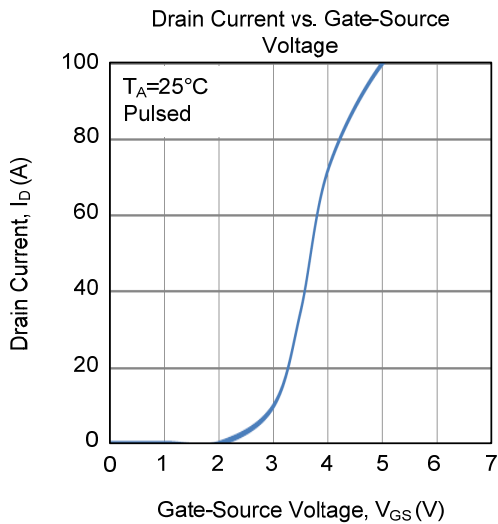
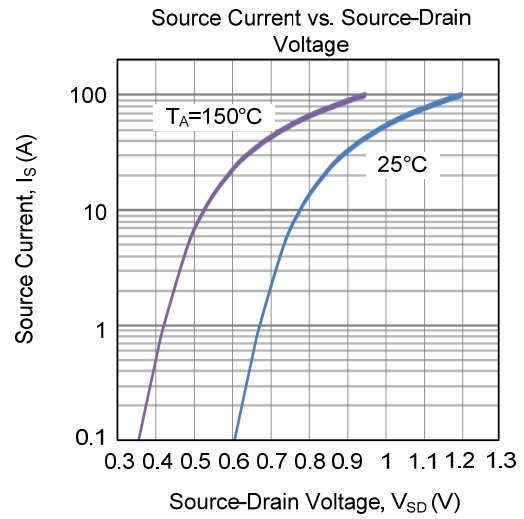
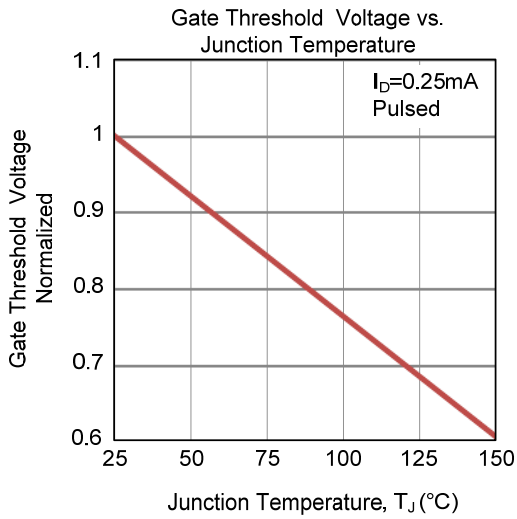


**Unclamped Inductive Switching Waveforms**

## TYPICAL CHARACTERISTICS

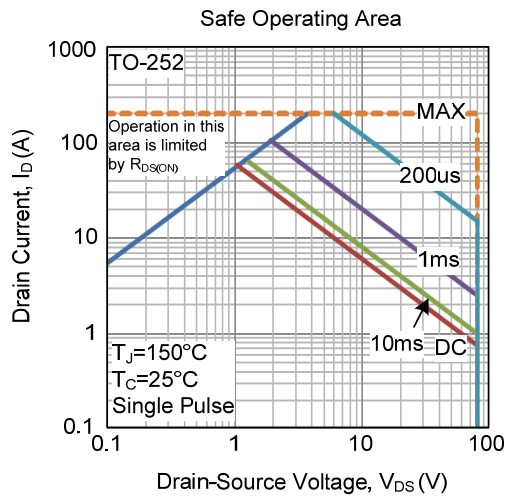


■ TYPICAL CHARACTERISTICS (Cont.)





■ TYPICAL CHARACTERISTICS (Cont.)



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