



U74HCT3G34

CMOS IC

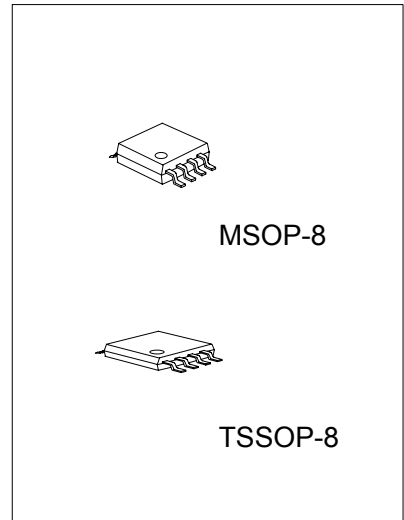
TRIPLE BUFFER GATE

DESCRIPTION

The U74HCT3G34 provides three buffers, it is compatible with TTL.

FEATURES

- * Low power dissipation
- * High speed
- * High noise immunity



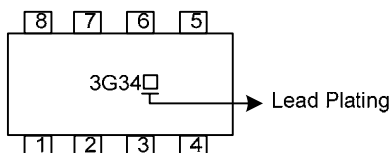
*Pb-free plating product number:
U74HCT3G34L

ORDERING INFORMATION

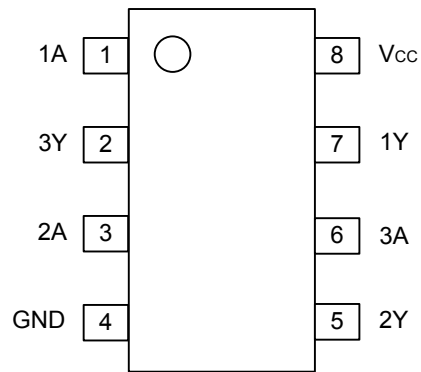
Ordering Number		Package	Packing
Normal	Lead Free Plating		
U74HCT3G34-P08-R	U74HCT3G34L-P08-R	TSSOP-8	Tape Reel
U74HCT3G34-P08-T	U74HCT3G34L-P08-T	TSSOP-8	Tube
U74HCT3G34-SM1-R	U74HCT3G34L-SM1-R	MSOP-8	Tape Reel
U74HCT3G34-SM1-T	U74HCT3G34L-SM1-T	MSOP-8	Tube

<p>U74HCT3G34L-P08-R</p> <p>(1) Packing Type (2) Package Type (3) Lead Plating</p>	<p>(1) R: Tape Reel, T: Tube (2) P08: TSSOP-8, SM1: MSOP-8 (3) L: Lead Free Plating, Blank: Pb/Sn</p>
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MARKING



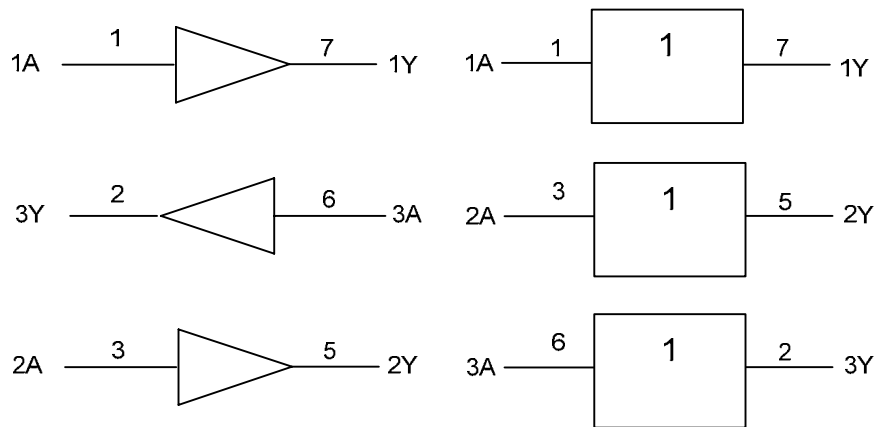
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT	OUTPUT
A	Y
L	L
H	H

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATINGS (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7	V
Output Voltage	V_{OUT}	-0.5~ $V_{CC}+0.5$	V
Output Current	I_{OUT}	25	mA
V_{CC} or GND Current	I_{CC}	50	mA
Input Clamp Current	I_{IK}	± 20	mA
Output Clamp Current	I_{OK}	± 20	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{STG}	-65 ~ +150	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Rise and Fall Times	t_R, t_F	$V_{CC}=4.5V$		6.0	500	ns
Operating Temperature	T_A		-40		+125	

■ STATIC CHARACTERISTICS ($T_A=25$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC}=4.5V\sim 5.5V$	2.0	1.6		V
Low-Level Input Voltage	V_{IL}	$V_{CC}=4.5V\sim 5.5V$		1.2	0.8	V
High-Level Output Voltage	V_{OH}	$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4	4.5		V
		$V_{CC}=4.5V, I_{OH}=-4.0mA$	4.13	4.32		V
Low-Level Output Voltage	V_{OL}	$V_{CC}=4.5V, I_{OL}=20\mu A$		0	0.1	V
		$V_{CC}=4.5V, I_{OL}=4.0mA$		0.15	0.33	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND			± 1.0	μA
Quiescent Supply Current	I_Q	$V_{CC}=5.5V, I_{OUT}=0, V_{IN}=V_{CC}$ or GND			10	μA
Additional Quiescent Supply Current	ΔI_Q	$V_{CC}=5.5V, V_{IN}=V_{CC}-2.1V; I_{OUT}=0$			375	μA
Input Capacitance	C_{IN}			1.5		pF

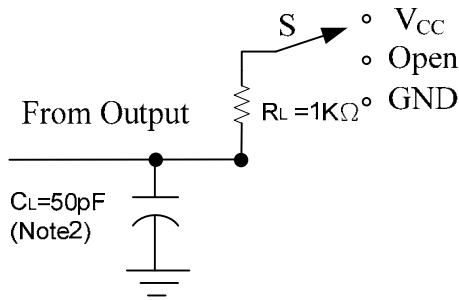
■ DYNAMIC CHARACTERISTICS ($T_A=25$, $t_R, t_F \leq 6.0ns$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From nA to nY	t_{PHL}/t_{PLH}	$V_{CC}=4.5V, C_L=50$ pF		10	23	ns
Output Transition Time	t_{THL}/t_{TLH}	$V_{CC}=4.5V, C_L=50$ pF		6	19	ns

■ OPERATING CHARACTERISTICS

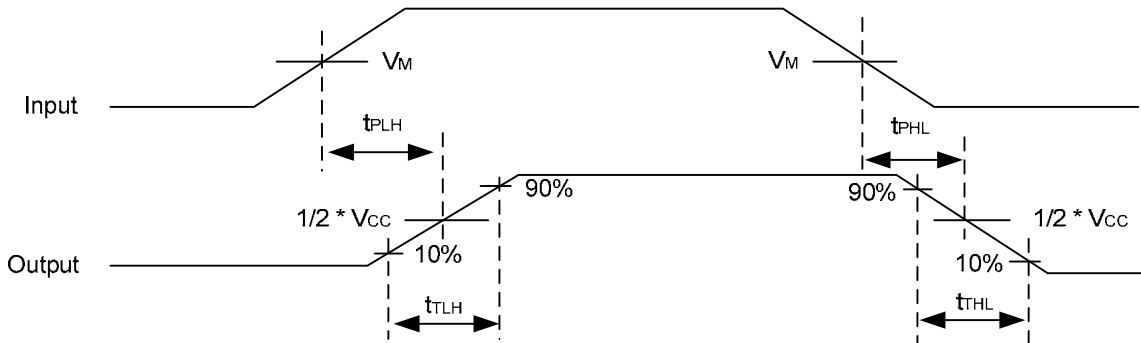
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance per Gate	C_{pd}			9		pF

■ T TEST CIRCUIT AND WAVEFORMS



TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{CC}

Note: C_L includes probe and jig capacitance.



$V_M=1.3V, Input=GND\ to\ 3.0V$

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