



U74LVC1G08

CMOS IC

2-INPUT AND GATE

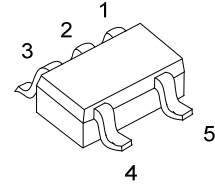
DESCRIPTION

The U74LVC1G08 is a 2-input AND gate which provides the Function $Y=A*B$.

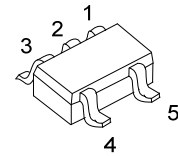
This device has power-down protective circuit to prevent device form destruction when it is powered down.

FEATURES

- * Inputs Accept Voltage up to 5.5V
- * Low Power Dissipation: $I_{CC}=10\mu A$ (Max)
- * $\pm 24mA$ Output Drive($V_{CC}=3.3V$)
- * Power Down Protection



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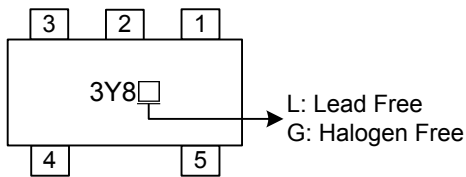
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ORDERING INFORMATION

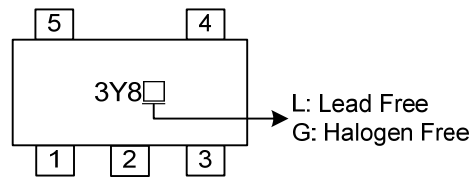
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC1G08L-AF5-R	U74LVC1G08G-AF5-R	SOT-25	Tape Reel
U74LVC1G08L-AL5-R	U74LVC1G08G-AL5-R	SOT-353	Tape Reel

<p>U74LVC1G08L-AF5-R</p> <p>(1) Packing Type (2) Package Type (3) Lead Plating</p>	<p>(1) R: Tape Reel (2) AF5: SOT-25, AL5: SOT-353 (3) G: Halogen Free, L: Lead Free</p>
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MARKING

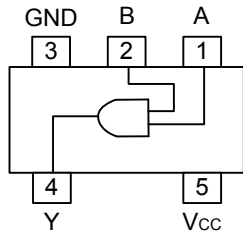


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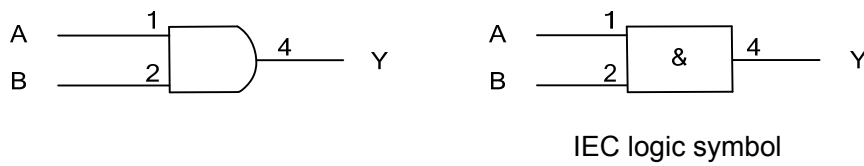
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~6.5	V
Input Voltage	V_{IN}	-0.5~6.5	V
Output Voltage(active mode)	V_{OUT}	-0.5~ $V_{CC}+0.5$	V
Output Voltage(power-down mode)	V_{OUT}	-0.5~6.5	V
Input Clamp Current($V_{IN}<0$)	I_{IK}	-50	mA
Output Clamp Current($V_{OUT}<0$)	I_{OK}	-50	mA
Output Current	I_{OUT}	±50	mA
V_{CC} or GND Current	I_{CC}	±100	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		85	°C

■ STATIC CHARACTERISTICS ($T_A=25^{\circ}C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC}=1.65V\sim 1.95V$	$0.65 \cdot V_{CC}$			V
		$V_{CC}=2.3V\sim 2.7V$	1.7			
		$V_{CC}=3.0V\sim 3.6V$	2			
		$V_{CC}=4.5V\sim 5.5V$	$0.7 \cdot V_{CC}$			
Low-Level Input Voltage	V_{IL}	$V_{CC}=1.65V\sim 1.95V$			$0.35 \cdot V_{CC}$	V
		$V_{CC}=2.3V\sim 2.7V$			0.7	
		$V_{CC}=3.0V\sim 3.6V$			0.8	
		$V_{CC}=4.5V\sim 5.5V$			$0.3 \cdot V_{CC}$	
High-Level Output Voltage	V_{OH}	$V_{CC}=1.65V \sim 5.5V, I_{OH}=-100\mu A$	$V_{CC}-0.1$			V
		$V_{CC}=1.65V, I_{OH}=-4mA$	1.2			
		$V_{CC}=2.3V, I_{OH}=-8mA$	1.9			
		$V_{CC}=3.0V, I_{OH}=-16mA$	2.4			
		$V_{CC}=3.0V, I_{OH}=-24mA$	2.3			
Low-Level Output Voltage	V_{OL}	$V_{CC}=1.65V \sim 5.5V, I_{OL}=100\mu A$			0.1	V
		$V_{CC}=1.65V, I_{OL}=4mA$			0.45	
		$V_{CC}=2.3V, I_{OL}=8mA$			0.3	
		$V_{CC}=3.0V, I_{OL}=16mA$			0.4	
		$V_{CC}=3.0V, I_{OL}=24mA$			0.55	
		$V_{CC}=4.5V, I_{OL}=32mA$			0.55	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0V \sim 5.5V, V_{IN}=5.5V$ or GND			±5	μA
Power OFF Leakage Current	I_{OFF}	$V_{CC}=0V, V_{IN}$ or $V_{OUT}=5.5V$			±10	μA
Quiescent Supply Current	I_Q	$V_{CC}=1.65V\sim 5.5V, V_{IN}=5.5V$ or GND $I_{OUT}=0$			10	μA
Additional Quiescent Supply Current	ΔI_Q	$V_{CC}=3V\sim 5.5V$, One input at $V_{CC}-0.6V$, other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_{IN}	$V_{CC}=3.3V, V_{IN}=V_{CC}$ or GND		4		pF

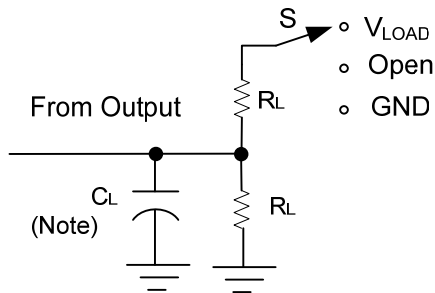
■ DYNAMIC CHARACTERISTICS (T_A=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (A or B) to output(Y)	t _{PLH} /t _{PHL}	V _{CC} =1.8V±0.15V, C _L =15pF	1.5		7.2	ns
		V _{CC} =2.5V±0.2V, C _L =15pF	0.7		4.4	ns
		V _{CC} =3.3V±0.3V, C _L =15pF	0.8		3.6	ns
		V _{CC} =5V±0.5V, C _L =15pF	0.8		3.4	ns
		V _{CC} =1.8V±0.15V, C _L =30 or 50pF	2.4		8	ns
		V _{CC} =2.5V±0.2V, C _L =30 or 50pF	1.1		5.5	ns
		V _{CC} =3.3V±0.3V, C _L =30 or 50pF	1		4.5	ns
		V _{CC} =5V±0.5V, C _L =30 or 50pF	1		4	ns

■ OPERATING CHARACTERISTICS (T_A=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Cpd	V _{CC} =1.8V, f=10MHz		21		pF
		V _{CC} =2.5V, f=10MHz		24		pF
		V _{CC} =3.3V, f=10MHz		26		pF
		V _{CC} =5V, f=10MHz		31		pF

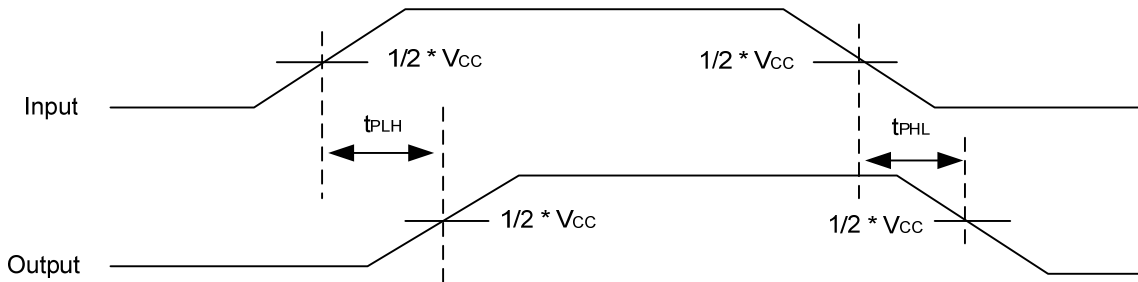
■ TEST CIRCUIT AND WAVEFORMS



TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{LOAD}

Note: C_L includes probe and jig capacitance.

V_{CC}	V_{IN}	t_R/t_F	V_M	V_{LOAD}	C_L	R_L	V_{Δ}
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 * V_{CC}$	15pF	1M Ω	0.15V
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 * V_{CC}$	15pF	1M Ω	0.15V
$3.3V \pm 0.3V$	3 V	$\leq 2.5ns$	1.5V	6V	15pF	1M Ω	0.3V
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	$2 * V_{CC}$	15pF	1M Ω	0.3V
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 * V_{CC}$	30pF	1K Ω	0.15V
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 * V_{CC}$	30pF	500 Ω	0.15V
$3.3V \pm 0.3V$	3 V	$\leq 2.5ns$	1.5V	6V	50pF	500 Ω	0.3V
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	$2 * V_{CC}$	50pF	500 Ω	0.3V



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