



## ULN2004

### LINEAR INTEGRATED CIRCUIT

## 7CH DARLINGTON SINK DRIVER

### DESCRIPTION

The UTC **ULN2004** are high-voltage, high-current darlington drivers comprised of seven NPN darlington pairs.

All units feature integral clamp diodes for switching inductive loads.

Applications include relay, hammer, lamp and display (LED) drivers.

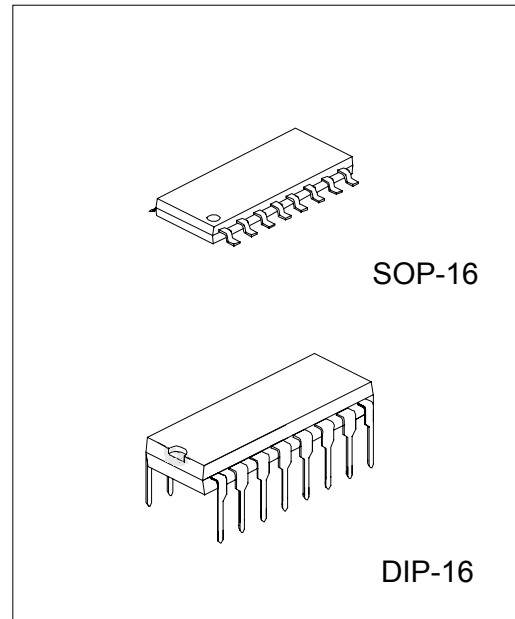
### FEATURES

\*Output current (single output): 500mA (MAX.)

\*High sustaining voltage output: 50V (MIN.)

\*Output clamp diodes

\*Inputs compatible with various types of logic

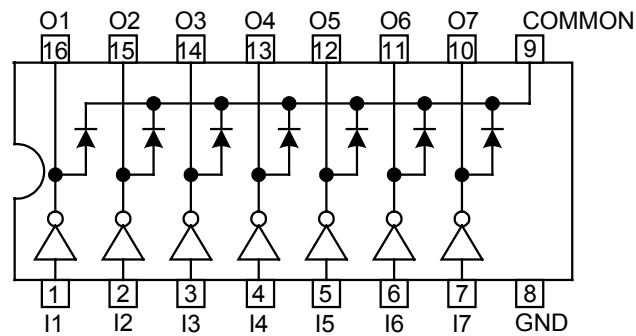


\*Pb-free plating product number: ULN2004L

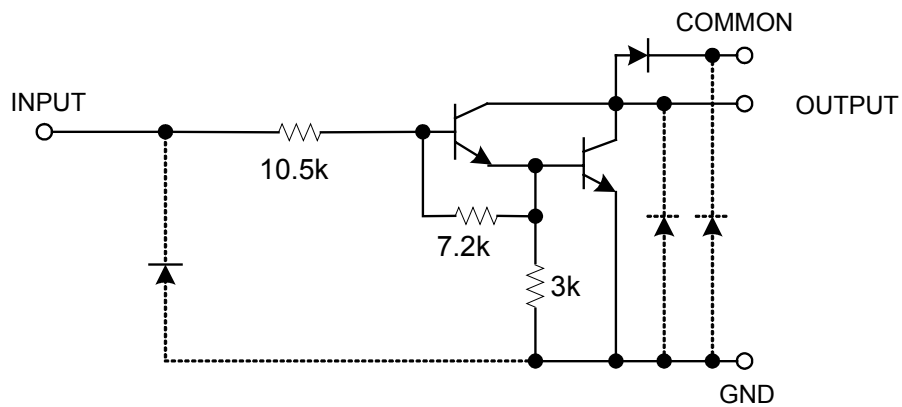
### ORDERING INFORMATION

Order Number		Package	Packing
Normal	Lead free plating		
ULN2004-S16-R	ULN2004L-S16-R	SOP-16	Tape Reel
ULN2004-S16-T	ULN2004L-S16-T	SOP-16	Tube
ULN2004-D16-T	ULN2004L-D16-T	DIP-16	Tube

## ■ PIN CONNECTION



## ■ BLOCK DIAGRAM



Note: The input and output parasitic diodes cannot be used as clamp diodes.

### ■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Output Sustaining Voltage	V <sub>OUT</sub>	-0.5~50	V
Output Current	I <sub>OUT</sub>	500	mA / ch
Input Voltage	V <sub>IN</sub>	-0.5~30	V
Clamp Diode Reverse Voltage	V <sub>R</sub>	50	V
Clamp Diode Forward Current	I <sub>F</sub>	500	mA
Power Dissipation	DIP-16	P <sub>D</sub>	1.47
	SOP-16		0.625
Junction Temperature	T <sub>J</sub>	+125	
Operating Temperature	T <sub>OPR</sub>	0~+70	
Storage Temperature	T <sub>STG</sub>	-40~+150	

Note 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The device is guaranteed to meet performance specification within 0 ~+70 operating temperature range and assured by design from -20 ~+85 .

### ■ RECOMMENDED OPERATING CONDITIONS (Ta=-40~+85 )

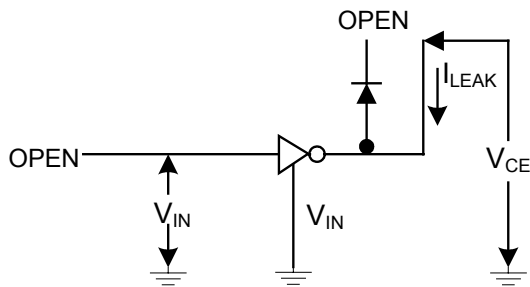
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Sustaining Voltage	V <sub>OUT</sub>		0		50	V
Output Current	I <sub>OUT</sub>	T <sub>pw</sub> = 25ms 7 Circuits Ta = 85 TJ = 120	Duty = 10%	0	370	mA/ch
			Duty = 50%	0	130	
			Duty = 10%	0	233	
			Duty = 50%	0	70	
Input Voltage	V <sub>IN</sub>		0		24	V
Input Voltage (Output On)	V <sub>IN(ON)</sub>	I <sub>OUT</sub> = 400mA, h <sub>FE</sub> = 800	6.2		24	V
Input Voltage (Output Off)	V <sub>IN(OFF)</sub>		0		1.0	V
Clamp Diode Reverse Voltage	V <sub>R</sub>				50	V
Clamp Diode Forward Current	I <sub>F</sub>				350	mA
Power Dissipation	DIP-16	P <sub>D</sub>	Ta = 85		0.76	W
	SOP-16		Ta = 85		0.325	

### ■ ELECTRICAL CHARACTERISTICS (Ta=25 unless otherwise specified)

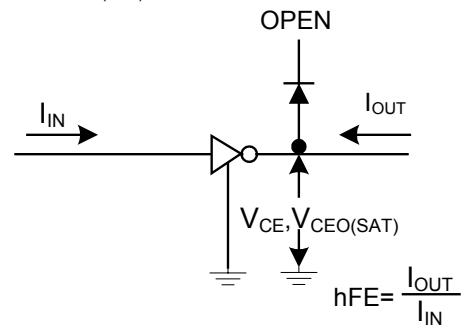
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Leakage Current	I <sub>LEAK</sub>	1	V <sub>CE</sub> = 50 V, Ta = 25			50	μA
			V <sub>CE</sub> = 50 V, Ta = 85			100	
Collector-Emitter Saturation Voltage	V <sub>CEO(SAT)</sub>	2	I <sub>OUT</sub> = 350 mA, I <sub>IN</sub> = 500 μA		1.3	1.6	V
			I <sub>OUT</sub> = 200 mA, I <sub>IN</sub> = 350 μA		1.1	1.3	
			I <sub>OUT</sub> = 100 mA, I <sub>IN</sub> = 250 μA		0.9	1.1	
DC Current Transfer Ratio	h <sub>FE</sub>	2	V <sub>CE</sub> = 2 V, I <sub>OUT</sub> = 350 mA	1000			
Input Current (Output On)	I <sub>IN(ON)</sub>	3	V <sub>IN</sub> = 9.5 V, I <sub>OUT</sub> = 350 mA		0.8	1.2	mA
Input Current (Output Off)	I <sub>IN(OFF)</sub>	4	I <sub>OUT</sub> = 500 μA, Ta = 85°C	50	65		μA
Input Voltage (Output On)	V <sub>IN(ON)</sub>	5	V <sub>CE</sub> = 2 V, I <sub>OUT</sub> = 350 mA			4.7	V
			h <sub>FE</sub> = 800, I <sub>OUT</sub> = 200 mA			4.4	
Clamp Diode Reverse Current	I <sub>R</sub>	6	V <sub>R</sub> = 50 V, Ta = 25°C			50	μA
			V <sub>R</sub> = 50 V, Ta = 85°C			100	
Clamp Diode Forward Voltage	V <sub>F</sub>	7	I <sub>F</sub> = 350 mA			2.0	V
Input Capacitance	C <sub>IN</sub>				15		pF
Turn-On Delay	t <sub>ON</sub>	8	V <sub>OUT</sub> = 50 V, R <sub>L</sub> = 125 Ω C <sub>L</sub> = 15 pF		0.1		μs
Turn-Off Delay	t <sub>OFF</sub>	8	V <sub>OUT</sub> = 50 V, R <sub>L</sub> = 125 Ω C <sub>L</sub> = 15 pF		0.2		

## ■ TEST CIRCUIT

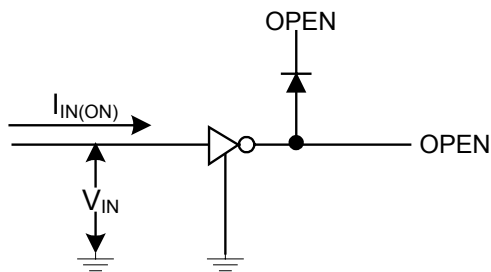
1.  $I_{LEAK}$



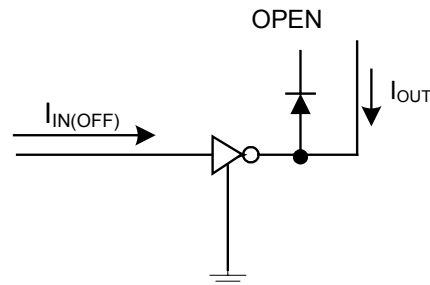
2.  $V_{CEO(SAT)}, h_{FE}$



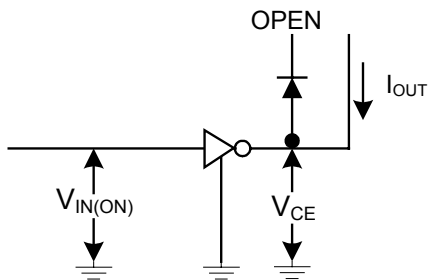
3.  $I_{IN(ON)}$



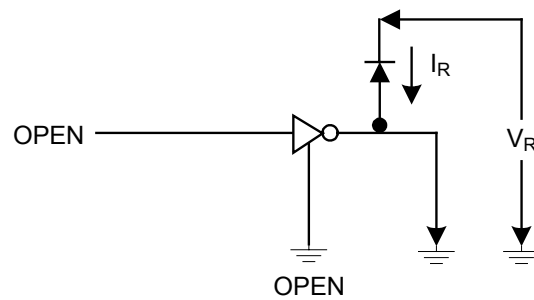
4.  $I_{IN(OFF)}$



5.  $V_{IN(ON)}$

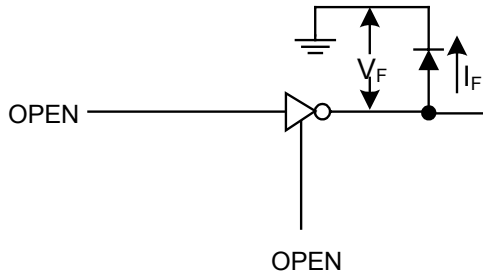


6.  $I_R$

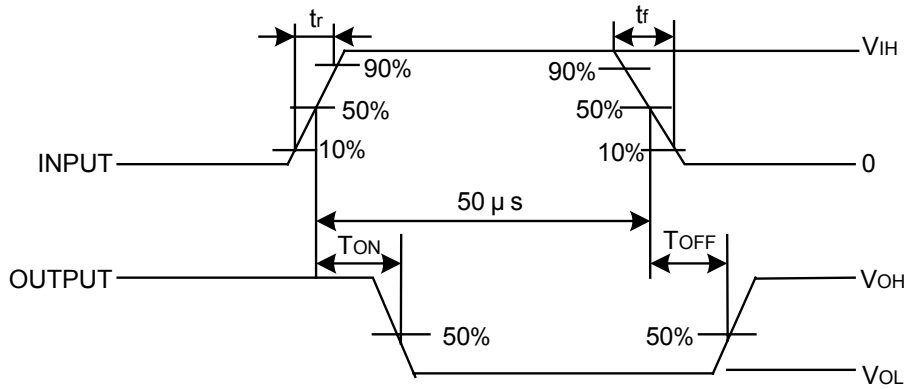
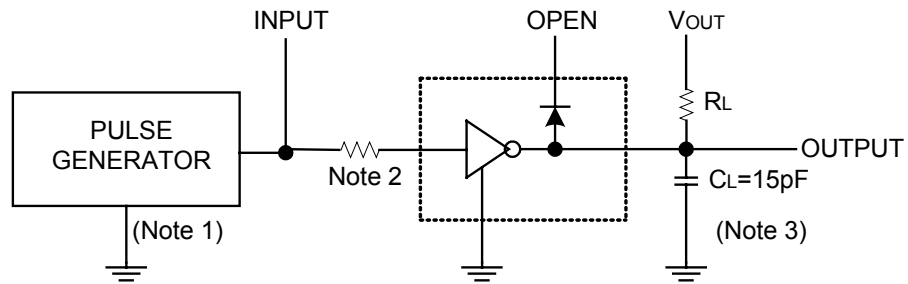


■ TEST CIRCUIT(cont.)

7.  $V_F$



8.  $t_{ON}$ ,  $t_{OFF}$



Note1: Pulse width 50  $\mu$ s ,duty cycle 10%  
Output impedance 50  $\Omega$  ,  $t_r$  5ns,  $t_f$  10ns

Note2: See below

INPUT CONDITION

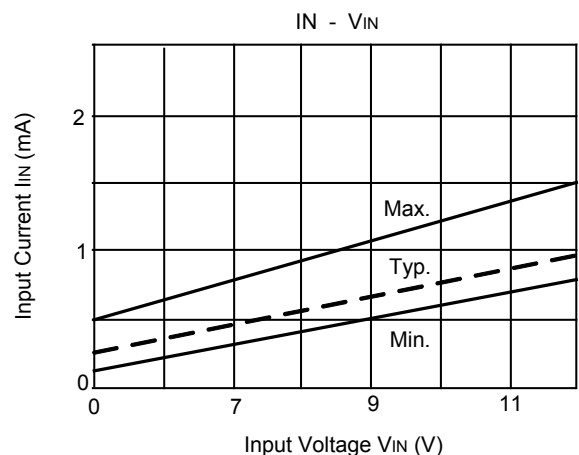
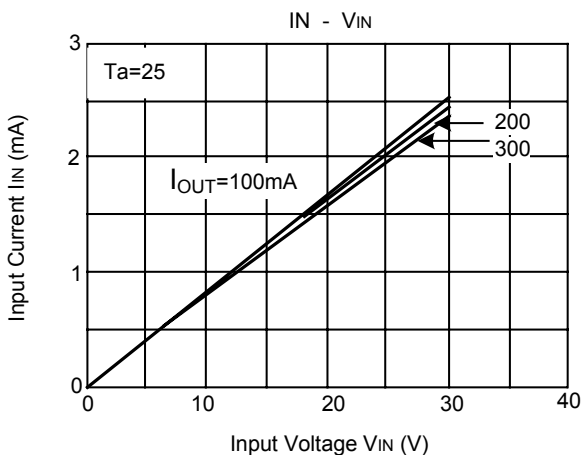
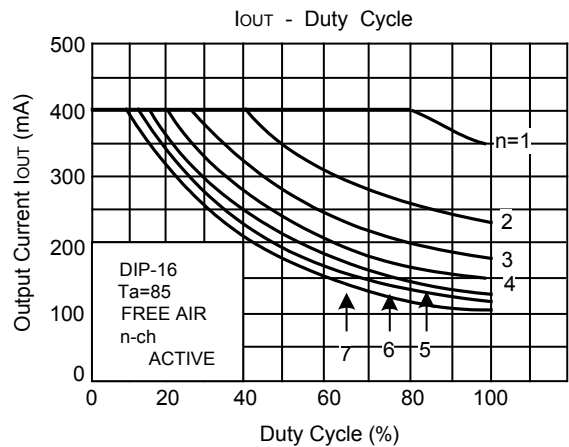
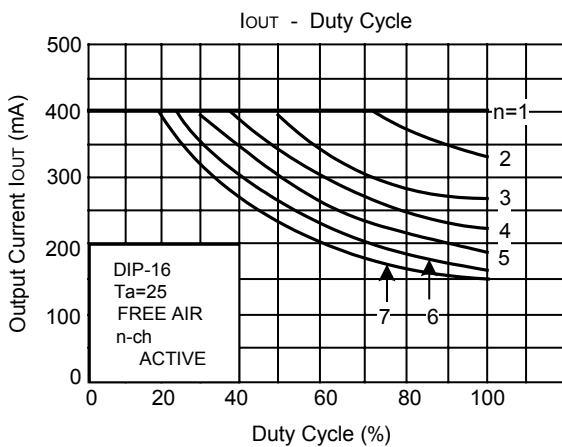
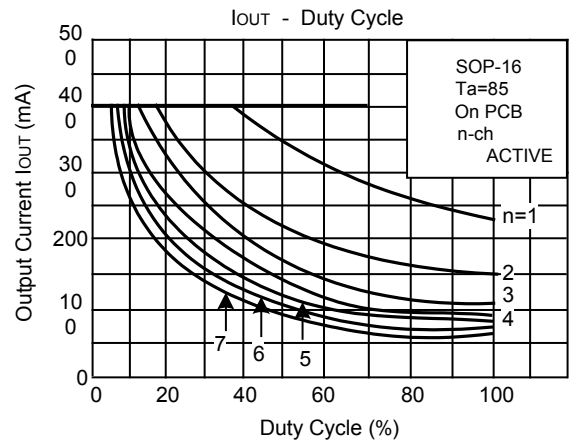
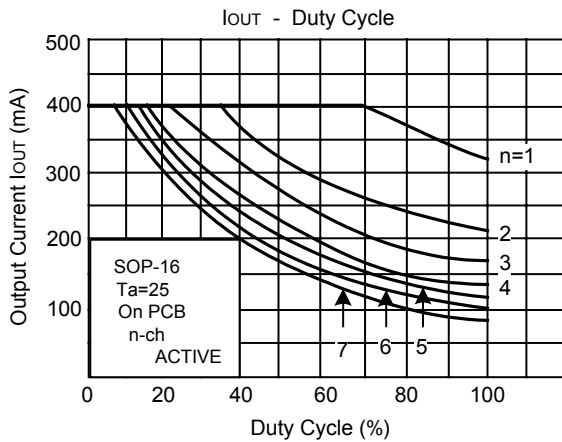
TYPE NUMBER	R1	$V_{IH}$
ULN2004	0	8V

Note3:  $C_L$  includes probe and jig capacitance

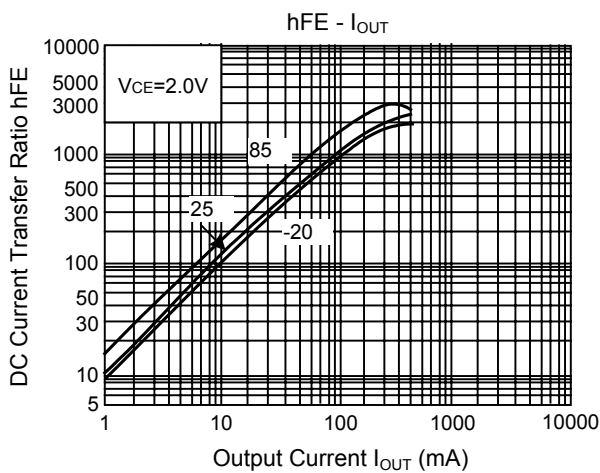
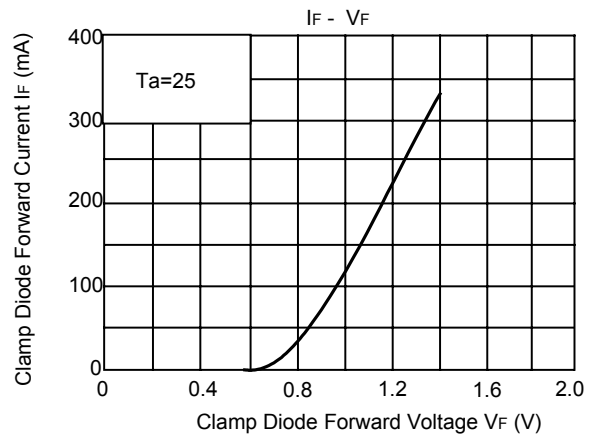
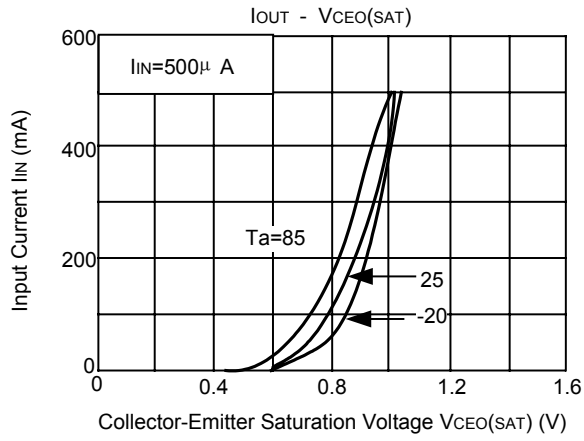
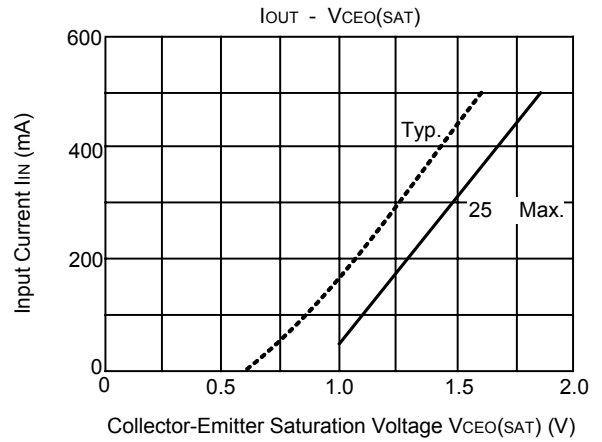
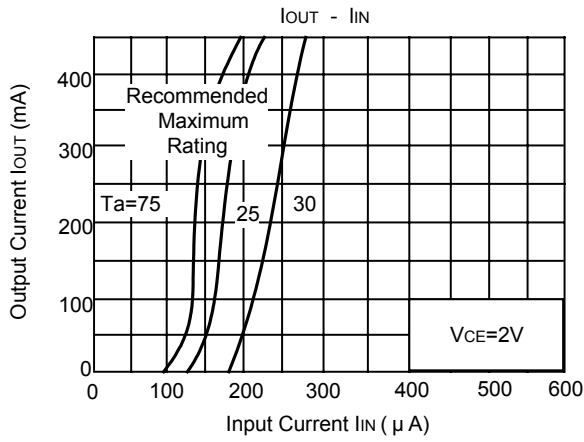
## ■ PRECAUTIONS FOR USING

This IC does not include built-in protection circuits for excess current or overvoltage. If this IC is subjected to excess current or overvoltage, it may be destroyed. Hence, the utmost care must be taken when systems which incorporate this IC are designed. Utmost care is necessary in the design of the output line, COMMON and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

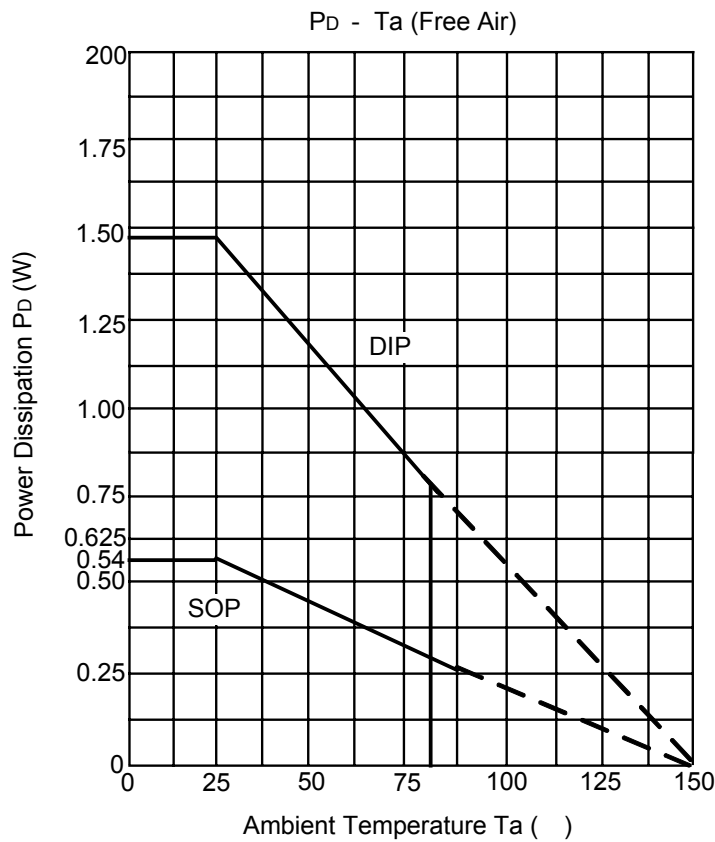
## ■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS(cont.)



■ TYPICAL CHARACTERISTICS(cont.)



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