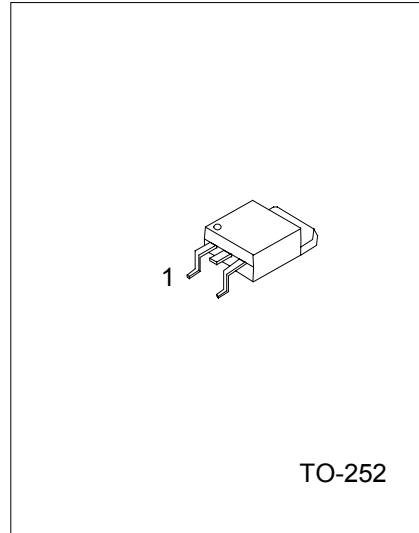
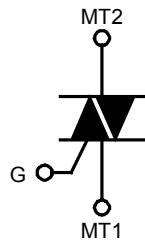


TRIACS

DESCRIPTION

Passivated triacs in a plastic envelope, suitable for surface mounting, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

SYMBOL



TO-252

1:MT1 2:MT2 3:GATE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Repetitive peak off-state voltages UT136F/G-5 UT136F/G-6 UT136F/G-8	V_{DRM}	500* 600* 800	V
RMS on-state current full sine wave, $T_{mb} \leq 107^\circ C$	$I_{T(RMS)}$	4	A
Non-repetitive peak on-state current (Full sine wave, $T_j = 25^\circ C$ prior to surge) $t = 20ms$ $t = 16.7 ms$	I_{TSM}	25 27	A
I^2t for fusing ($t = 10 ms$)	I^2t	3.1	A^2s
Repetitive rate of rise of on-state current after triggering $I_{TM} = 6 A, I_G = 0.2A, diG/dt = 0.2A/\mu s$ T2+ G+ T2+ G- T2- G- T2- G+	diT/dt	50 50 50 10	$A/\mu s$
Peak gate voltage	V_{GM}	5	V
Peak gate current	I_{GM}	2	A
Peak gate power	P_{GM}	5	W
Average gate power (over any 20 ms period)	$P_{G(AV)}$	0.5	W
Storage temperature	T_{stg}	-40 ~ 150	$^\circ C$
Operating junction temperature	T_j	125	$^\circ C$

*Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed $3A/\mu s$.

THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal resistance, Junction to mounting base	R _{th j-mb}			3.0	K/W
Full cycle				3.7	
Thermal resistance, Junction to ambient Pcb mounted	R _{th j-a}		75		K/W

STATIC CHARACTERISTICS (T_j=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX		UNIT
					UT136F	UT136G	
Gate trigger current	I _{GT}	V _D =12V, I _T =0.1A T2+ G+ T2+ G- T2- G- T2- G+		5	25	50	mA
				8	25	50	
				11	25	50	
				30	70	100	
Latching current	I _L	V _D =12V, I _{GT} =0.1A T2+ G+ T2+ G- T2- G- T2- G+		7	20	30	mA
				16	30	45	
				5	20	30	
				7	30	45	
Holding current	I _H	V _D = 12 V, I _{GT} = 0.1 A		5	15	30	mA
On-state voltage	V _T	I _T =5A		1.4	1.70		V
Gate trigger voltage	V _{GT}	V _D =12V, I _T =0.1A		0.7	1.5		V
		V _D =400V, I _T =0.1A, T _j =125°C	0.25	0.4			V
Off-state leakage current	I _D	V _D =V _{DRM(max)} , T _j =125°C		0.1	0.5		mA

DYNAMIC CHARACTERISTICS (T_j=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN		TYP	MAX	UNIT
			UT136F	UT136G			
Critical rate of rise of Off-state voltage	dV _D /dt	V _{DM} = 67% V _{DRM(max)} , T _j =125°C, exponential waveform, gate open circuit	50	200	250		V/μs
Critical rate of change of Commutating voltage	dV _{com} /dt	V _{DM} =400V, T _j =95°C, I _{T(RMS)} =4A, dI _{com} /dt =1.8A/ms, gate open circuit		10	50		V/μs
Gate controlled turn-on time	t _{gt}	I _{TM} = 6 A, V _D = V _{DRM(max)} , I _G =0.1A, dI _G /dt=5A/μs			2		μs

TYPICAL CHARACTERISTICS

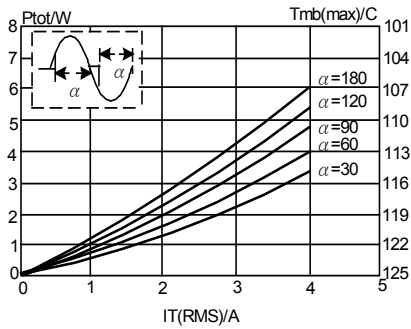


Fig. 1. Maximum on-state dissipation, P_{tot} vs rms on-state current, $I_T(RMS)$ where α = conduction angle.

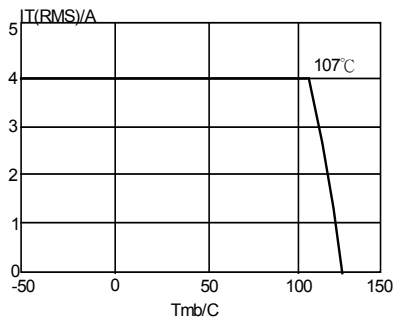


Fig. 4. Maximum permissible rms current $I_T(RMS)$ vs mounting base temperature T_{mb}

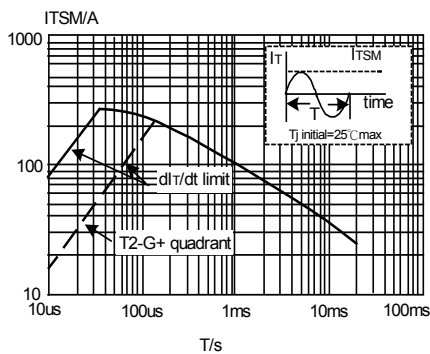


Fig. 2. Maximum Permissible non-repetitive peak on-state Current I_{TSM} vs pulse width t_p , for sinusoidal currents, $t_p \leq 20ms$

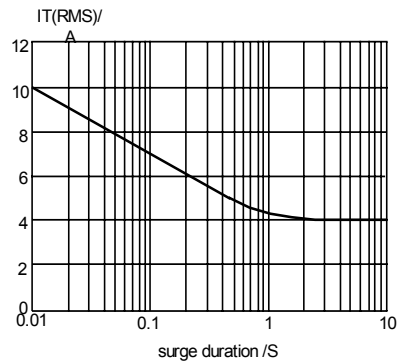


Fig. 5. Maximum permissible repetitive rms on-state current $I_T(RMS)$, vs surge duration, for sinusoidal currents, $f=50Hz$; $T_{mb} \leq 107^\circ C$

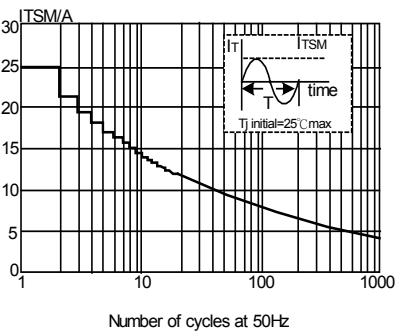


Fig. 3. Maximum Permissible non-repetitive peak on-state current I_{TSM} , vs number of cycles, for sinusoidal currents, $f=50Hz$.

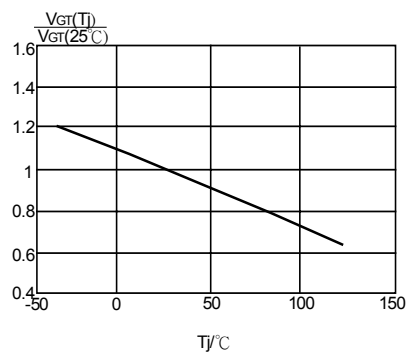


Fig. 6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^\circ C)$, vs junction temperature T_j .

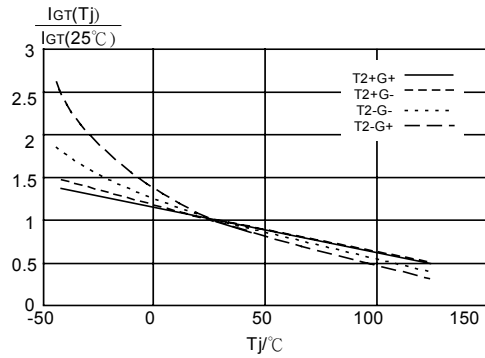


Fig. 7. Normalised gate trigger Current $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$, vs junction temperature T_j

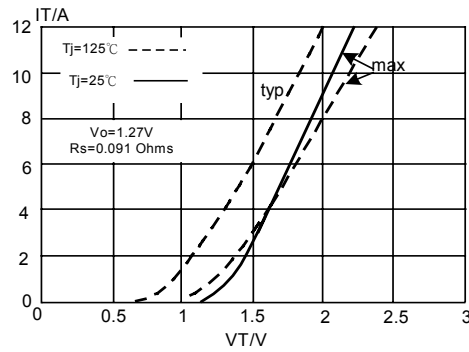


Fig. 10. Typical and maximum on-state characteristic.

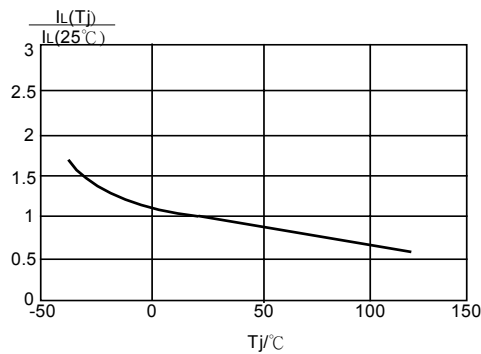


Fig. 8. Normalised latching Current $I_L(T_j)/I_L(25^\circ\text{C})$, vs junction temperature T_j

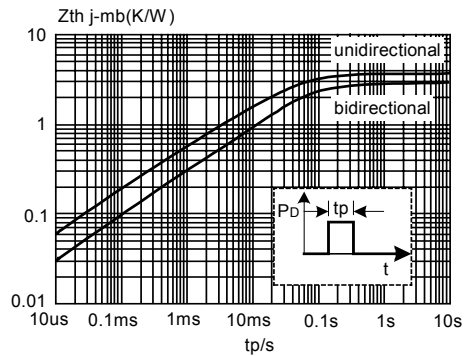


Fig. 11. Transient thermal impedance Z_{thj-mb} , vs pulse width t_p .

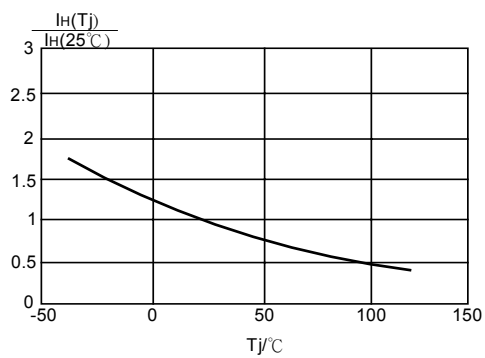


Fig. 9. Normalised holding current $I_H(T_j)/I_H(25^\circ\text{C})$, vs junction temperature T_j

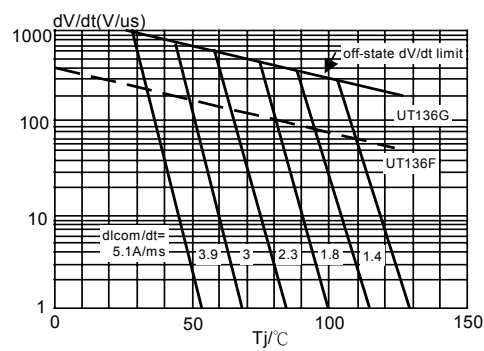


Fig. 12. Typical commutation dV/dt vs junction temperature, parameter commutation dI/dt . The triac should commute when the dV/dt is below the value on the appropriate curve for pre-commutation dI/dt

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