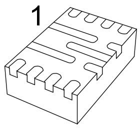
6.0A, 30V, 500KHZ/1.1MHZ SYNCHRONOUS STEP-DOWN CONVERTER



VQFN-13(2×3)

■ DESCRIPTION

The UTC **UD30600** is a fully integrated easy to use synchronous step-down Buck converter, which integrated low on resistance high-side and low-side power MOSFETs.

The **UD30600** can deliver 6A of output current efficiently with constant on time (COT) control for fast loop response. The **UD30600** can select frequency and work mode by FM pin, for achieving high efficiency at light load, the device can work at PFM mode, IC also can work at FPWM mode to achieve small output ripple with full load range.

The **UD30600** has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, output over voltage protection, FB open protection and thermal shutdown in case of excessive power dissipation.

■ FEATURES

* Wide 3.6V to 30V Input Range
* Support 6A Continuous Output Current
* 500kHz/1.1MHz Switching Frequency Selectable
* Low $R_{DS(ON)}$ for Internal Switches:
  High-side:32mΩ
  Low-side: 20mΩ
* PFM and FPWM Mode Selectable
* Constant On Time Control for Fast Loop Response l
* Support Up to 100% Duty Cycle
* Power good inductor
* Output Discharge
* Output Voltage Adjustable from 0.6V
* Support Pre-Biased Output Startup
* Full Protection, OCP, OVP, OTP, SCP, FB Open Protection

■ APPLICATIONS

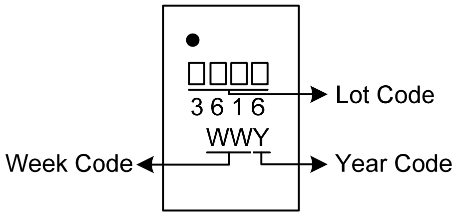
* Telecom and Networking Systems
* Home Appliance and White goods
* IP Camera
* Multi-functional Printer
* Industrial Control
* General Purpose Point-of-Load (POL)

■ ORDERING INFORMATION

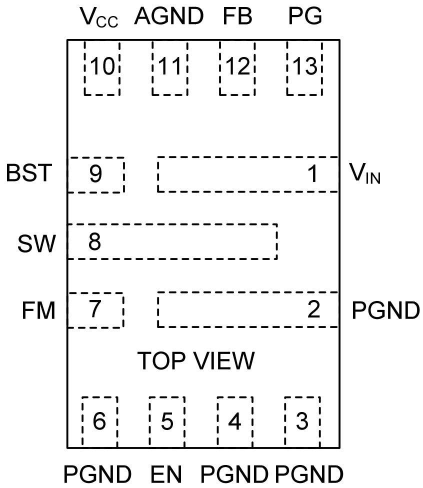
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UD30600L-QAP-R	UD30600G-QAP-R	VQFN-13(2×3)	Tape Reel

UD30600G-QAP-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) QAP: VQFN-13(2×3) (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



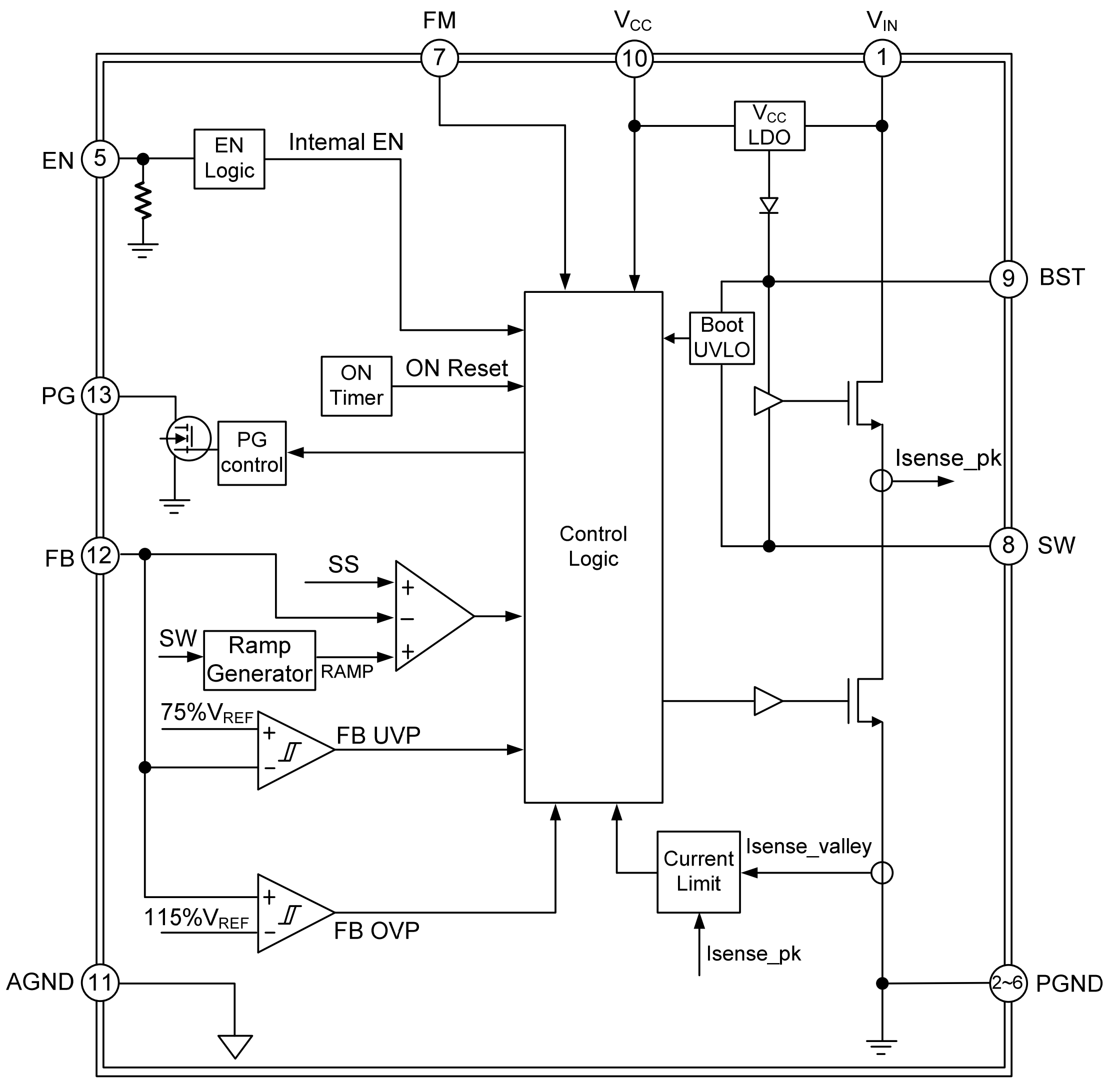
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{IN}	**Input Supply Pin.** V_{IN} supplies the internal bias LDO and drain of the internal high-side FET. Place a capacitor (CIN) as close as to the IC as possible to prevent large voltage spikes from appearing at the input.
2,3,4,6	PGND	**Power Ground terminal.** PGND is the reference ground of the regulated output voltage. Use wide PCB traces to make the connection.
5	EN	**Enable pin of Buck.** Pull high to enable Buck. Pull to GND or Float this pin to disable Buck.
7	FM	**Operation mode and frequency selection.** Program FM to select CCM, pulse skip mode, and the operating switching frequency. Connect a resistor between FM pin and GND can configure the frequency.
8	SW_N	**Switching output of the convertor.** Internally connected to source of the high-side FET and drain of the low-side FET of Buck. Connect to power inductor.
9	BST	**Bootstrap pin.** Connect a capacitor between SW and BST pins to form a floating supply across the High-side switch driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
10	V_{CC}	**Internal 5V LDO regulator output.** Decouple V_{CC} with a 1Mf capacitor. The V_{CC} LDO is shutdown when EN is pulled low.
11	AGND	**Analog ground.** Connect AGND to PGND.
12	FB	**Feedback input to the convertor of Buck.** Connect a resistor divider to set the output voltage.
13	PG	**Power Good Indicator.** Open drain structure. Need connect to an external voltage source through a pull-up resistor (e.g. 100kΩ). Floating it if not used.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
V_{IN} to PGND	V_{IN}	-0.3 ~ 31	V
EN to PGND	EN	-0.3 ~ 31	V
SW to PGND	SW	-0.7 (-5V in 10ns) ~ V_{IN} + 0.7	V
BST to SW	BST	-0.3 ~ 6	V
All Other Pins		-0.3 ~ 6	V
Operating Junction Temperature	T_J	-40 ~ +150	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
V_{IN} to PGND	V_{IN}	3.6 ~ 30	V
V_{OUT} to PGND	V_{OUT}	0.6 ~ V_{IN}	V
Max. Continuous Output Current	I_{OUT}	6	A

■ THERMAL DATA (NOTE)

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	32	°C/W
Junction to Case	θ_{JC}	8	°C/W

Note: Device mounted on 4-Layer PCB, 64mm x 64mm board.

■ ELECTRICAL CHARACTERISTICS (V_{IN}=12V, V_{EN}=2V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT UVLO AND QUIESCENT CURRENT						
V_{IN} UVLO Rising Threshold	V_{CC_UVR}			3.25		V
V_{IN} UVLO Falling Threshold	V_{CC_UVF}			2.95		V
Shutdown Supply Current	I_{QS}	V_{IN} = 12V		1	3	μA
Quiescent Supply Current	I_Q	No Load, V_{FB} = 0.7V, No switching		350		μA
EN						
Enable Rising Threshold	V_{EN_R}	Low to high		1.2		V
Enable Falling Threshold	V_{EN_F}	High to low		1.05		V
Enable Input Resistor	R_{EN}	V_{EN} = 2V		2400		kΩ
V_{CC} REGULATOR						
V_{CC} Regulator	V_{CC}	V_{IN} > 5.2V		5		V
V_{CC} Current Limit	I_{VCC}	High to Low	20			mA
BUCK FEEDBACK VOLTAGE						
Feedback Voltage	V_{FB}	T_J = 25°C	591	600	609	mV
Feedback Leakage	I_{LK_FB}	V_{FB} = 2V			0.1	μA
BUCK HIGH SIDE AND LOW SIDE MOSFETs						
High-Side Switch on Resistance	R_{ON_HS}	V_{BST} - V_{SW} = 5V		32		mΩ
Low-Side Switch on Resistance	R_{ON_LS}	V_{IN} = 12V		20		mΩ
High-Side Leakage	LKG_{HS}	V_{EN} = 0V, V_{SW} = 0V			1	μA
Low-Side Leakage	LKG_{LS}	V_{EN} = 0V, V_{SW} = 18V			1	μA
OUTPUT DISCHARGE RESISTOR						
	$R_{DISCHARGE}$			200		Ω
BUCK CURRENT LIMIT						
Low-Side Valley Current Limit	I_{LIM_LS}			7		A
High-Side Peak Current Limit	I_{LIM_HS}			8.5		A
Negative Current Limit	I_{NOC}			-4		A
BUCK OUTPUT OVP AND UVP						
Output OVP Rising Threshold	$V_{OVP\_rising\_th}$			115%		V_{FB}
Output OVP Falling Threshold	$V_{OVP\_falling\_th}$			105%		V_{FB}
Output UVP Falling Threshold	$V_{UVP\_falling\_th}$			75%		V_{FB}
Output UVP Rising Threshold	$V_{UVP\_rising\_th}$			85%		V_{FB}
POWER GOOD INDUCTOR						
Output OVP Rising Threshold	$PG_{OVP\_rising\_th}$			115%		V_{FB}
Output OVP Falling Threshold	$PG_{OVP\_falling\_th}$			105%		V_{FB}
Output UVP Falling Threshold	$PG_{UVP\_falling\_th}$			80%		V_{FB}
Output UVP Rising Threshold	$PG_{UVP\_rising\_th}$			85%		V_{FB}
	P_{G_Delay}			100		μS
SOFT START						
Soft-Start Time	T_{SS}	V_O from 10% to 90%		4.5		mS
SWITCHING FREQUENCY						
Oscillator Frequency	F_{SW}	R_{FM} = GND, PFM		500		KHz
		R_{FM} = 36kΩ, PFM		1100		KHz
		R_{FM} = 270kΩ, FPWM		1100		KHz
		R_{FM} = Float, FPWM		500		KHz
Minimum Switch ON Time	T_{ON_MIN}			70		nS
Minimum Switch OFF Time	T_{OFF_MIN}			240		nS
FB UV Hiccup	F_{B_UV}			75%		V_{FB}
Thermal Shutdown Rising Threshold	T_{OTP_R}			160		°C
Thermal Shutdown Falling Threshold	T_{OTP_F}			130		°C

■ FUNCTION DESCRIPTIONS

Pulse-Width Modulation (PWM) Control

The **UD30600** is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

Heavy-Load Operation

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps (see Figure 1). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the next period begins. In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode

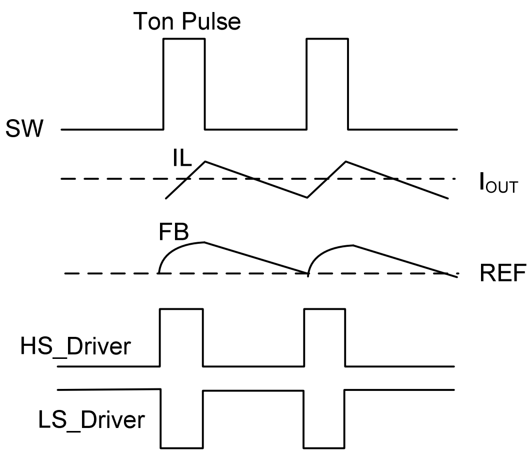


Figure 1.FPWM Operation

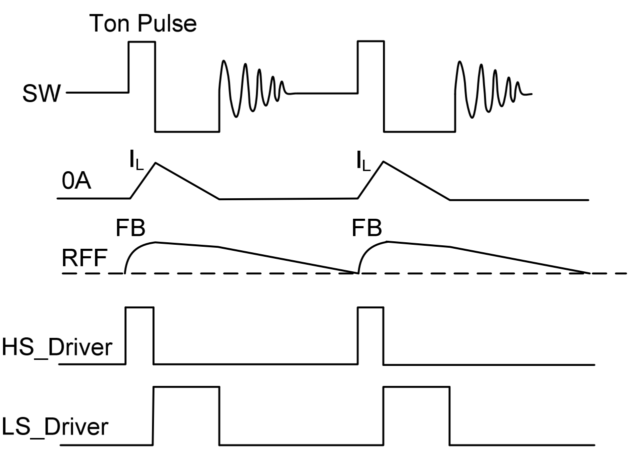


Figure 2.PFM Operation

■ FUNCTION DESCRIPTIONS (Cont.)

Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load operation is shown in Figure 2. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, V_{FB} cannot reach V_{REF} while the inductor current is approaching zero. The LS-FET driver enters tri-state (Hi-Z) whenever the inductor current reaches zero. The output capacitors discharge to GND through the LS-FET slowly. As a result, the efficiency in light-load condition is improved greatly. In light-load condition, the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode.

At light-load or no-load condition, the output drops very slowly, and the **UD30600** reduces the switching frequency naturally. High efficiency is achieved at light load.

As the output current increases from the light-load condition, the current modulator regulation time period becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation:

$$I_{OUT}\_Critical=\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{2\times L_{OUT}\times F_{SW}\times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Under-Voltage Lockout (UVLO) Protection

The **UD30600** has under-voltage lockout (UVLO) protection: the part starts up only when V_{CC}/V_{IN} exceed UVLO rising thresholds (3.25V typically). The part shuts down when the V_{IN}/V_{CC} voltage is lower than the UVLO falling threshold voltage (typically 2.95V), the UVLO protection is non-latch off.

EN Control

EN is used to enable or disable the entire chip. Pull EN high (>1.2V typically) to turn on the regulator. Pull EN low(<1.05V typically) to turn off the regulator. For automatic start-up, EN can be pulled up to the input voltage through a resistive voltage divider or directly to V_{IN}. To determine the automatic start-up voltage, calculate the values of the pull-up resistor (RUP from V_{IN} to EN) and the pull-down resistor (RDOWN from EN to GND) with Equation

$$V_{IN\_Start}=\frac{1.2V\times(R_{UP}+R_{DOWN})}{R_{DOWN}} \quad (2)$$

If an application requires a higher UVLO, use EN to adjust the input voltage UVLO by using two external resistors (see Figure 3).

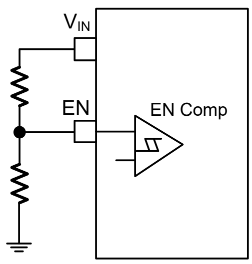


Figure 3. Adjustable UVLO Application Circuits

■ FUNCTION DESCRIPTIONS (Cont.)

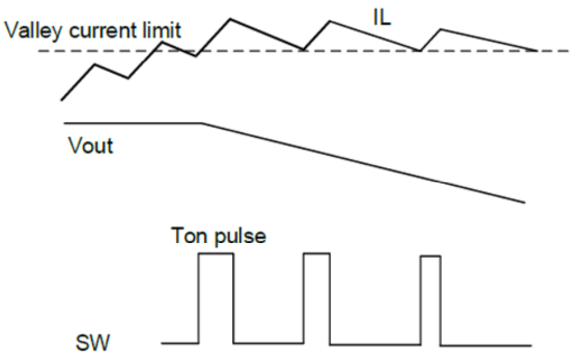
Power Good inductor

The **UD30600** uses a power-good (PG) output to indicate whether the output voltage of the buck regulator ready or not. PG is the open drain of a MOSFET and should be connected to another voltage source through a resistor (e.g. 100kΩ~500kΩ). Once the input voltage is applied, and the internal feedback voltage reaches 85% of internal V_{REF}, PG will be pulled high after a delay time (100µs typically). When V_{FB} drops to 80% of internal V_{REF} PG will be pulled low. While the feedback voltage rises up to 115% of internal V_{REF}, PG will be pulled low too, once FB drops below 105% pf V_{REF}, PG will active high again.

PG has self-bias function, if V_{IN} is absent, even PG pulled up by external power source, PG will be pulled down internally.

Over-Current Limit (OCL)

The **UD30600** has a valley current-limit control. During LS-FET on, the inductor current is monitored. If the current is higher than valley current limit, the LS limit compactor active. The device enters over current protection mode. High side will not be turned on until the valley current limit disappear. Meanwhile, the output voltage drops until V_{FB} is below the under voltage (UV) threshold (typically 25% of the reference). Once UV is triggered, the **UD30600** enters hiccup mode to restart the part periodically. During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.



Fiqure 4. Valley Current limit control

Since the comparison is done during the LSFET on state, the OC trip level sets the valley level of the inductor current. The maximum load current at the over-current threshold (IOC) can be calculated with Equation:

$$I_{OC}=I_{LIMIT}+\frac{\Delta Iinductor}{2} \quad (3)$$

Output OVP

The **UD30600** monitors a resistor-divided V_{FB} to detect over-voltage. When V_{FB} becomes higher than 115% of the target voltage, the over-voltage protection (OVP) comparator output goes high, and the circuit will turn on the low side MOSFET to discharge the output. LSFET will turned off until the negative current limit is triggered then LSFET will remain off for 5us to turn on again. IC will repeat this behavior until the output OVP condition is removed.

■ FUNCTION DESCRIPTIONS (Cont.)

FM Select Frequency/Mode Programmable

The **UD30600** can setup the operation mode and PWM frequency by connecting FM pin to GND with a resistor. Below table shows the configuration.

Table 1. Frequency and Mode configuration

R_{FM} (kΩ)	Work Mode	Frequency(kHz)
0	PFM	500
36	PFM	1100
270	FPWM	1100
Float	FPWM	500

Large Duty Cycle Operation

When **UD30600** will automatically extend the frequency to support the application when V_{IN} is close to V_{OUT}. The frequency extend circuit will be triggered when T_{OFF} min time is reached. The **UD30600** can support up to 100% maximum duty cycle. 100% duty cycle operation will be disabled when OC is triggered.

Thermal Shutdown

Thermal shutdown is employed in the **UD30600**. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 160°C), the converter shuts off. This is a non-latched protection. There is a hysteresis of about 30°C. Once the junction temperature drops to about 130°C, a soft start is initiated.

Output Discharge

During the EN off period, the output is discharging via a 200Ω resistor on the SW. This discharge FET will be turned off when V_{OUT} is fully discharged or the 10ms timer is finished.

■ APPLICATION INFORMATION

The **UD30600** output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.6V. The feedback network is shown below Figure 6.

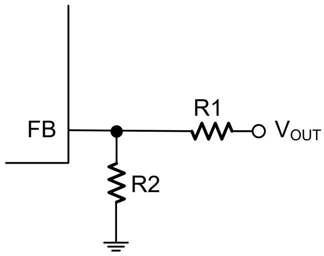


Figure 5. Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT}=V_{FB}\times\frac{R1+R2}{R2} \tag{4}$$

Selecting the Inductor

For most applications, use a 2.2μH to 10μH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, use an inductor with a small DC resistance. For most designs, the inductance value can be derived from Equation:

$$L=\frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times\Delta I_L\times f_{SW}} \tag{5}$$

Where ΔI_L is the inductor ripple current.

Selecting Input capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the V_{IN} pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$C_{IN}=I_{OUT}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \tag{6}$$

The worse case occurs at V_{IN} = 2V_{OUT}, where:

$$I_{CIN}=\frac{I_{OUT}}{2} \tag{7}$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimated as follows:

$$\Delta V_{IN}=\frac{I_{OUT}}{F_{OSC}\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \tag{8}$$

Under worse case where V_{IN} = 2V_{OUT}:

$$\Delta V_{IN}=\frac{1}{4}\times\frac{I_{OUT}}{F_{OSC}\times C_{IN}} \tag{9}$$

■ APPLICATION INFORMATION (Cont.)

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as: The output capacitor maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times F_{OSC}\times C_{OUT}}\right) \tag{10}$$

Where L is the inductor value, and RESR is the equivalent series resistance (ESR) value of the output capacitor, FOSC is the switching frequency. Note that, in real application, should consider that the ceramic capacitor capacitance has derating.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. The output voltage ripple caused by ESR is very small. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(\frac{1}{8\times F_{OSC}\times C_{OUT}}\right) \tag{11}$$

In the case of Electronic capacitors (e.g. Polymer or POSCAP capacitors), the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR} \tag{12}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The **UD30600** can be optimized for a wide range of capacitance and ESR values. In most of applications, Polymer capacitor is highly recommended due to the lower ESR performance. Besides considering the output ripple, chose larger output capacitor also can get better load transient response, but maximum output capacitor limitation should be also considered in design application. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{OUT_max} can be limited approximately by:

$$C_{OUT\_MAX}=\left(I_{LIMITave}-I_{OUT}\right)\times T_{SS}/V_{OUT} \tag{13}$$

Where, I_{LIM_AVG} is the average start-up current during soft-start period, T_{SS} is the soft-start time (4.5ms typically).

Table 2 lists the recommended feedback resistor values for common output voltages.

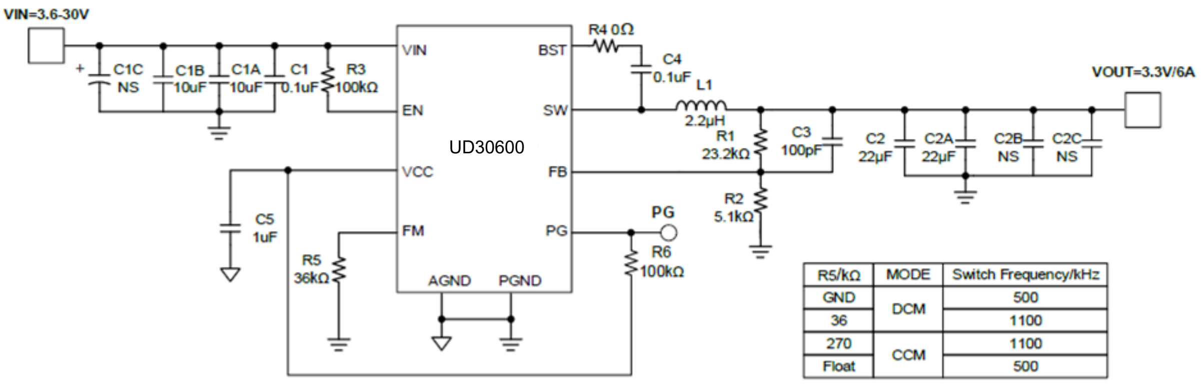
Table 2. Resistor Selection for Common Output Voltages (Note 1, 2)

V_{OUT} (V) (Note 2)	R1 (kΩ)	R2 (kΩ)	C3 (pF)	Lout (μH)	C_{OUT} (μF)
1	3.4	5.1	100	1	22 x 2
1.2	5.1	5.1	100	1	22 x 2
1.5	7.68	5.1	100	1	22 x 2
1.8	10.2	5.1	100	1.5	22 x 2
2.5	16.2	5.1	100	1.5	22 x 2
3.3	23.2	5.1	100	2.2	22 x 2
5	37.9	5.1	100	3.3	22 x 2
12	97.6	5.1	33	3.3	22 x 3

Notes: 1. For a detailed design circuit, please refer to the Typical Application Circuits.
2. The table recommends parameters based on F_{SW}=1.1MHz.

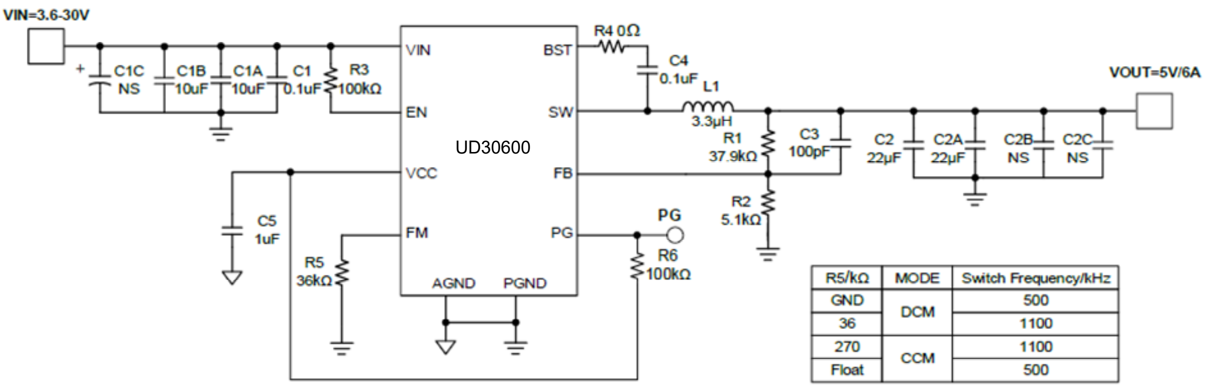
■ TYPICAL APPLICATION CIRCUIT

V_{OUT}=3.3V/6A, 1.1MHz



R5/kΩ	MODE	Switch Frequency/kHz
GND	DCM	500
36		1100
270	CCM	1100
Float		500

V_{OUT}=5V/6A, 1.1MHz



R5/kΩ	MODE	Switch Frequency/kHz
GND	DCM	500
36		1100
270	CCM	1100
Float		500