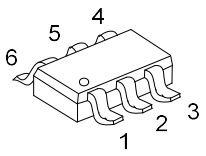
UESD5V0U4U06

ESD / TVS

LOW CAPACITANCE ESD PROTECTION ARRAY FOR HIGH SPEED DATA INTERFACES



SOT-26

■ DESCRIPTION

The UTC **UESD5V0U4U06** is a high performance and low cost design which includes surge rated diode arrays to protect high speed data interfaces. The UTC UESD5V0U4U06 family has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

The UTC **UESD5V0U4U06** is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

The UTC **UESD5V0U4U06** may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (± 15kV air, ±8kV contact discharge).

■ FEATURES

* ESD protection for 4 high-speed I/O lines and 1 V_{DD} line
* Provide ESD protection for each channel to
  IEC 61000-4-2 (ESD) ±27kV (air), ±17kV (contact)
  IEC 61000-4-5 (Lightning) 10A (8/20μs)
* Low capacitance : 1.26 pF typical
* Fast turn-on and Low clamping voltage
* Array of surge rated diodes with internal equivalent TVS diode
* Small package saves board space
* Solid-state silicon-avalanche and active circuit triggering technology
* Green & Pb Free

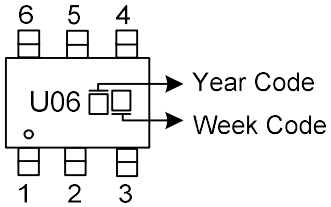
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■ ORDERING INFORMATION

Ordering Number	Package	Packing
UESD5V0U4U06G-AG6-R	SOT-26	Tape Reel

UESD5V0U4U06G-AG6-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AG6: SOT-26 (3) G: Halogen Free and Lead Free

■ MARKING



■ MARKING INFORMATION

W: Year Code

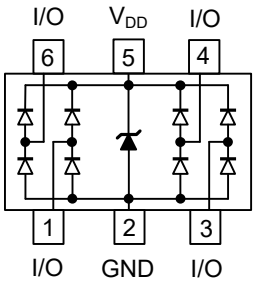
DATE	2XX0	2XX1	2XX2	2XX3	2XX4	2XX5	2XX6	2XX7	2XX8	2XX9
CODE	0	1	2	3	4	5	6	7	8	9

D: Week Code

Week	1	2	3	4	5	6	7	8	9	10	11	12
CODE	A	B	C	D	E	F	G	H	J	K	L	M
Week	13	14	15	16	17	18	19	20	21	22	23	24
CODE	N	P	Q	R	S	T	U	V	W	X	Y	Z
Week	25	26	27	28	29	30	31	32	33	34	35	36
CODE	5	6	7	8	9	A	B	C	D	E	F	G
Week	37	38	39	40	41	42	43	44	45	46	47	48
CODE	H	J	K	L	M	N	P	Q	R	S	T	U
Week	49	50	51	52	53							
CODE	V	W	X	Y	Z							

Note: Weeks 30 to 53 are marking with underlines.

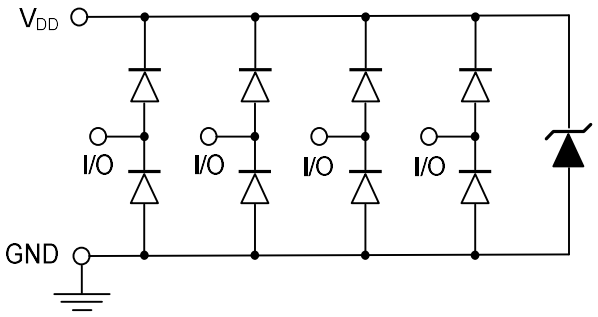
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	I/O	Terminal of ESD 1
2	GND	Ground
3	I/O	Terminal of ESD 2
4	I/O	Terminal of ESD 3
5	V_{DD}	Supply Voltage
6	I/O	Terminal of ESD 4

■ CIRCUIT DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
ESD Discharge	IEC61000-4-2	Air Discharge	V_{ESD}	±27	kV
		Contact Discharge		±17	kV
Peak Pulse Current	IEC61000-4-5	t_p=8/20μs	I_{PP}	10	A
Peak Pulse Power			P_{PP}	100	W
Operating Supply Voltage (V_{DD}-GND)			V_{DC}	6	V
DC Voltage at Any I/O Pin			V_{IO}	(GND – 0.5) to (V_{DD} + 0.5)	V
Operating Temperature			T_{OPR}	-55 ~ +85	°C
Storage Temperature			T_{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

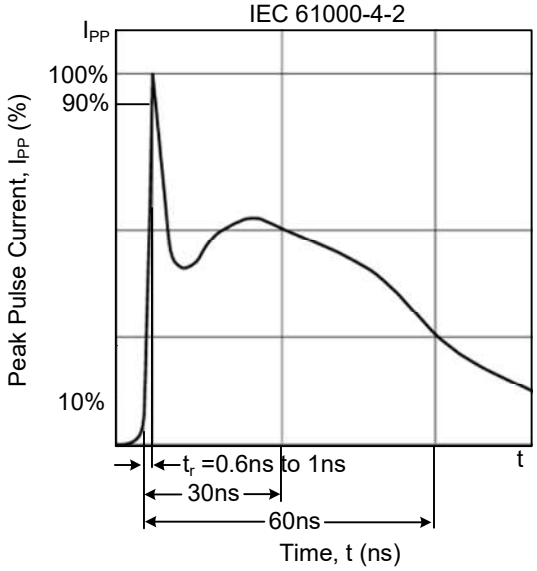
■ ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reverse Stand-Off Voltage	V_{RWM}	Pin 5 to Pin 2, T_A=25°C			5	V
Reverse Leakage Current	I_{Leak}	V_{RWM}=5V, Pin 5 to Pin 2			5	μA
Channel Leakage Current	$I_{CH-Leak}$	V_{PIN5}=5V, V_{PIN2}=0V			1	μA
Reverse Breakdown Voltage	V_{BR}	I_R=1mA, T_A=25°C, Pin 5 to Pin 2	5		8	V
Forward Voltage	V_F	I_F=15mA, GND to Any Pin		0.8	1.2	V
Lightning Clamping Voltage	$V_{CL-I/O}$	I_{PP}=5A, t_P=8/20μs, Any Channel pin to Ground		8		V
	$V_{CL--VDD}$	I_{PP}=5A, t_P=8/20μs, V_{DD} pin to Ground		7		V
Dynamic Resistance (Note 1)	R_{DYN}	Any I/O PIN to GND		0.3		Ω
	R_{DYN}	V_{DD} PIN to GND		0.16		Ω
Channel Input Capacitance	C_{IN}	V_{PIN5}=Floated, V_{PIN2}=0V, V_{IN}=2.5V, f=1MHz, Any Channel pin to Ground		1.26	2.3	pF
Channel Input Capacitance	ΔC_{IN}	V_{PIN5}=Floated, V_{PIN2}=0V, V_{IN}=2.5V, f=1MHz, Channel_x pin to Ground - Channel_y pin to Ground		0.02	0.08	pF

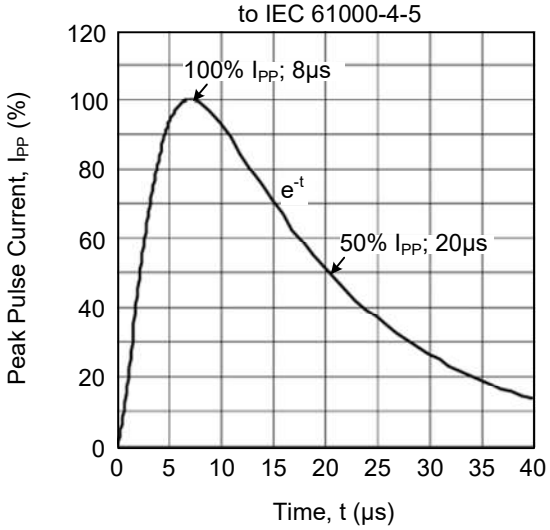
Notes: 1. TLP Parameter: Z_0=50Ω, t_p=100ns, t_r=2ns, Averaging Window from 60ns to 80ns. R_{DYN} is Calculated from 4A to 16A.

■ TYPICAL CHARACTERISTICS

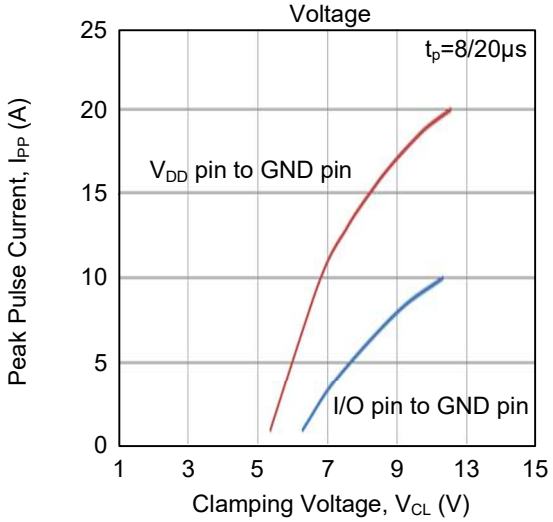
ESD pulse waveform according to IEC 61000-4-2



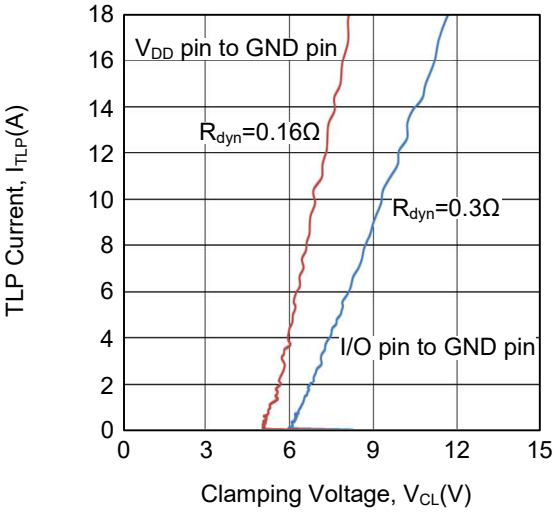
8/20 μs pulse waveform according to IEC 61000-4-5



Peak Pulse Current vs. Clamping Voltage



Clamping Voltage(TLP)



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