



UMC31

Preliminary

NPN SILICON TRANSISTOR

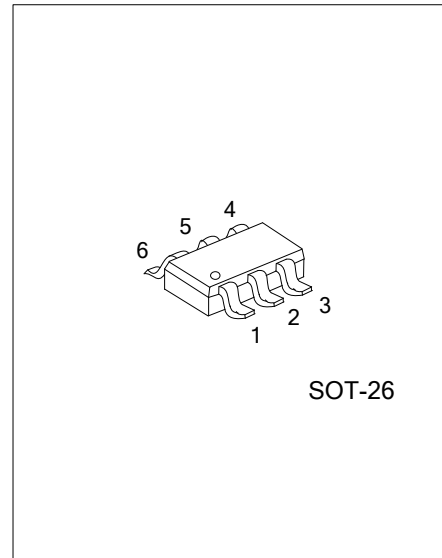
DUAL DIGITAL TRANSISTOR (BUILT- IN BIAS RESISTORS)

DESCRIPTION

The UTC **UMC31** is an dual transistor; it uses UTC's advanced technology to provide the customers with low collector -emitter saturation voltage, etc.

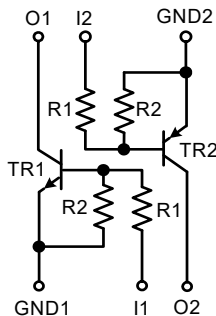
FEATURES

- * Both the DTB113Z chip and DTD113Z chip in a SOT-26 package.
- * NPN/PNP silicon transistor(Built-in resistor type)
- * Low collector-emitter saturation voltage
- * With built-in bias resistors
- * Simplify circuit design



SOT-26

EQUIVALENT CIRCUIT



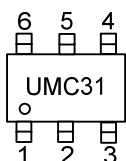
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment						Packing
Lead Free	Halogen Free		1	2	3	4	5	6	
UMC31L-AG6-R	UMC31G-AG6-R	SOT-26	G1	I1	O2	G2	I2	O1	Tape Reel

Note: Pin Assignment: G: GND I: IN O: OUT

UMC31G-AG6-R	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) AG6: SOT-26
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ ABSOLUTE MAXIMUM RATING ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS		UNIT
		TR1 (NPN)	TR2 (PNP)	
Supply Voltage	V_{CC}	50	-50	V
Input Voltage	V_{IN}	-5 ~ +10	-10 ~ +5	V
Output Current	I_{OUT}	500	-500	mA
Power Dissipation	P_C	420		mW
Junction Temperature	T_J	+150		$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150		$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	298	$^{\circ}\text{C/W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

TR1 (NPN)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	$V_{IN(OFF)}$	$V_{CC}=5V, I_{OUT}=100\mu A$			0.3	V
	$V_{IN(ON)}$	$V_{OUT}=0.3V, I_{OUT}=20mA$	1.5			V
Collector Cut-off Current	I_{CBO}	$V_{CB}=50V$			100	nA
Collector Cut-off Current	I_{CEO}	$V_{CE}=50V$			0.5	μA
Output Voltage	$V_{OUT(ON)}$	$I_{OUT}/I_{IN}=50mA/2.5mA$		0.1	0.3	V
Input Current	I_{IN}	$V_{IN}=5V$			7.2	mA
Output Current	$I_{OUT(OFF)}$	$V_{CC}=50V, V_{IN}=0V$			0.5	μA
DC Current Gain	h_{FE}	$V_{OUT}=5V, I_{OUT}=50mA$	82			
Input Resistance	R_1		0.7	1	1.3	K Ω
Resistor Ratio	R_2/R_1		8	10	12	
Transition Frequency	f_T	$V_{CE}=10V, I_E=-50mA, f=100MHz$ (Note)		200		MHz

Note: Transition frequency of the device.

TR2 (PNP)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	$V_{IN(OFF)}$	$V_{CC}=-5V, I_{OUT}=-100\mu A$			-0.3	V
	$V_{IN(ON)}$	$V_{OUT}=-0.3V, I_{OUT}=-20mA$	-3			V
Output Voltage	$V_{OUT(ON)}$	$I_{OUT}/I_{IN}=-50mA/-2.5mA$			-0.3	V
Input Current	I_{IN}	$V_{IN}=-5V$			-7.2	mA
Output Current	$I_{OUT(OFF)}$	$V_{CC}=-50V, V_{IN}=0V$			-0.5	μA
DC Current Gain	h_{FE}	$V_{OUT}=-5V, I_{OUT}=-50mA$	50			
Input Resistance	R_1		0.7	1	1.3	K Ω
Resistance Ratio	R_2/R_1		8	10	12	
Transition Frequency	f_T	$V_{CE}=-10V, I_E=50mA, f=100MHz$ (Note)		200		MHz

Note: Transition frequency of the device.

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