



## UT100N07H

Preliminary

Power MOSFET

### 100A, 70V N-CHANNEL POWER MOSFET

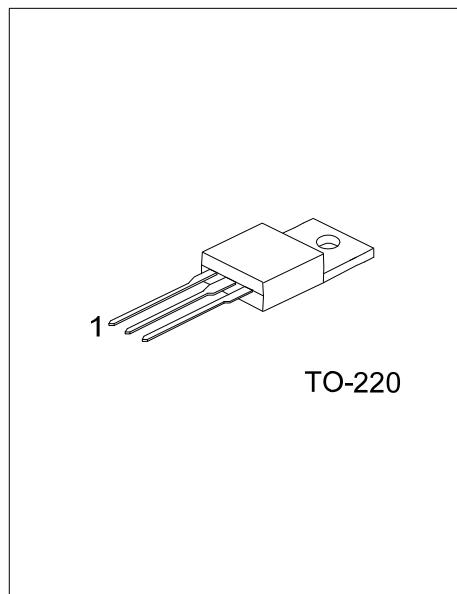
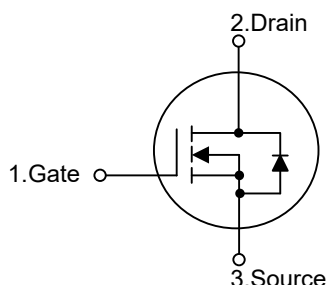
#### DESCRIPTION

The UTC **UT100N07H** is an N-channel enhancement mode Power FET, it uses UTC's advanced technology to provide customers a minimum on-state resistance and high switching speed.

#### FEATURES

- \*  $R_{DS(ON)} \leq 7.0 \text{ m}\Omega$  @  $V_{GS}=10\text{V}$ ,  $I_D=50\text{A}$
- \* High switching speed
- \* Improved dv/dt capability

#### SYMBOL



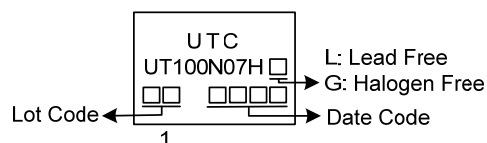
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT100N07HL-TA3-T	UT100N07HG-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

UT100N07HG-TA3-T	(1) Packing Type (2) Package Type (3) Green Package	(1) T: Tube (2) TA3: TO-220 (3) G: Halogen Free and Lead Free, L: Lead Free
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#### MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DS}$	70	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	Continuous	$I_D$	100	A
	Pulsed	$I_{DM}$	200	A
Avalanche Energy	Single Pulsed	$E_{AS}$	125	mJ
Peak Diode Recovery $dv/dt$ (Note 4)		$dv/dt$	2.5	V/ns
Power Dissipation		$P_D$	200	W
Junction Temperature		$T_J$	+150	$^{\circ}\text{C}$
Storage Temperature Range		$T_{STG}$	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $L = 0.1\text{mH}$ ,  $I_{AS} = 50\text{A}$ ,  $V_{DD} = 30\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^{\circ}\text{C}$

4.  $I_{SD} \leq 30\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	$\theta_{JA}$	62.5	$^{\circ}\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	0.625	$^{\circ}\text{C}/\text{W}$

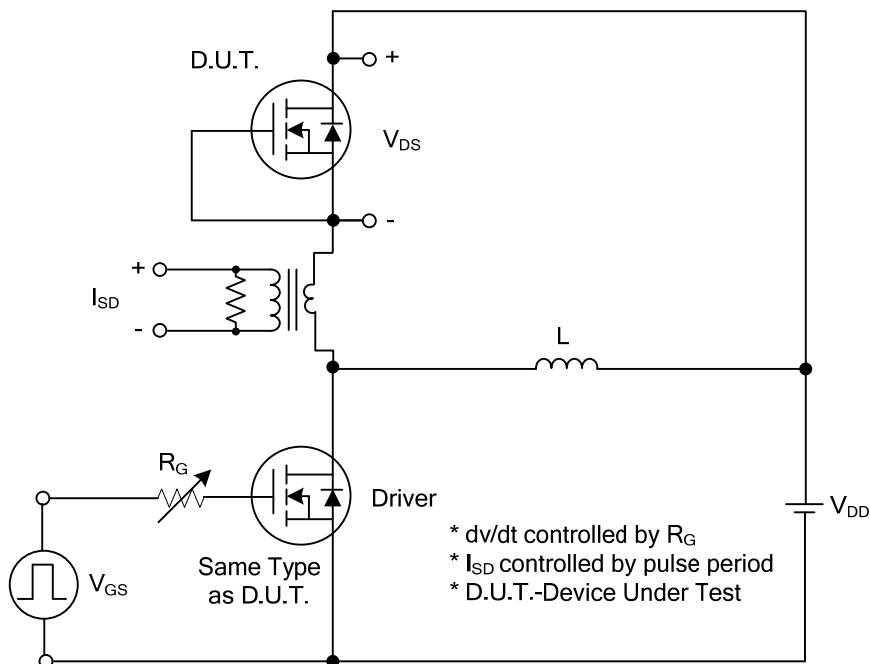
■ ELECTRICAL CHARACTERISTICS ( $T_J=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	70			V
Drain-Source Leakage Current		I <sub>DSS</sub>	V <sub>DS</sub> =70V, V <sub>GS</sub> =0V			1	μA
Gate-Source Leakage Current	Forward	I <sub>GSS</sub>	V <sub>GS</sub> =+20V, V <sub>DS</sub> =0V			+100	nA
	Reverse		V <sub>GS</sub> =-20V, V <sub>DS</sub> =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V <sub>GS(TH)</sub>	I <sub>D</sub> =250μA, V <sub>DS</sub> =V <sub>GS</sub>	2.0		4.0	V
Static Drain-Source On-State Resistance		R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =50A			7.0	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		14300		pF
Output Capacitance		C <sub>OSS</sub>			1460		pF
Reverse Transfer Capacitance		C <sub>RSS</sub>			1270		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q <sub>G</sub>	V <sub>DD</sub> =56V, V <sub>GS</sub> =10V, I <sub>D</sub> =100A, (Note 1, 2)		145		nC
Gate to Source Charge		Q <sub>GS</sub>			40		nC
Gate to Drain Charge		Q <sub>GD</sub>			60		nC
Turn-ON Delay Time		t <sub>D(ON)</sub>	V <sub>DD</sub> =35V, V <sub>GS</sub> =10V I <sub>D</sub> =100A, R <sub>G</sub> =3Ω (Note 1, 2)		18		ns
Rise Time		t <sub>R</sub>			19		ns
Turn-OFF Delay Time		t <sub>D(OFF)</sub>			34		ns
Fall-Time		t <sub>F</sub>			20		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I <sub>S</sub>				100	A
Maximum Body-Diode Pulsed Current		I <sub>SM</sub>				200	A
Drain-Source Diode Forward Voltage		V <sub>SD</sub>	I <sub>S</sub> =100A			1.4	V
Reverse Recovery Time		t <sub>rr</sub>	I <sub>S</sub> =30A, V <sub>GS</sub> =0V		60		nS
Reverse Recovery Charge (Note 1)		Q <sub>rr</sub>	dI <sub>r</sub> /dt=100A/μs		105		nC

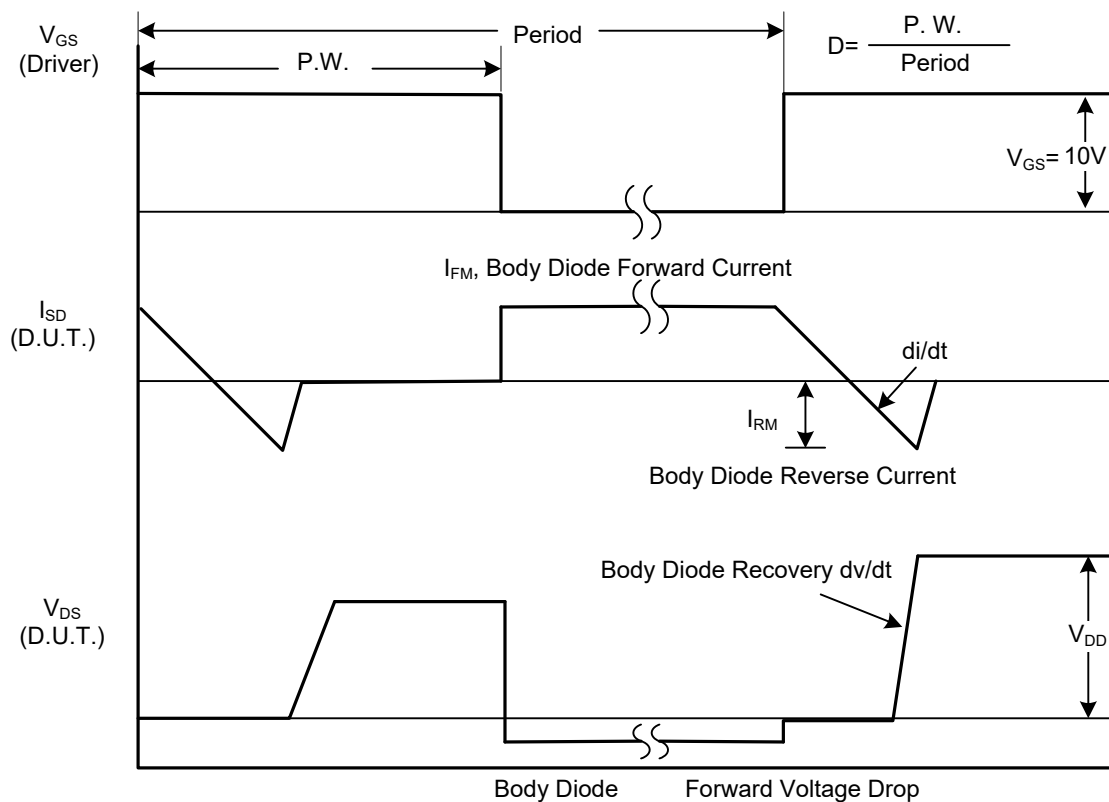
Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .

2. Essentially independent of operating ambient temperature.

### ■ TEST CIRCUITS AND WAVEFORMS

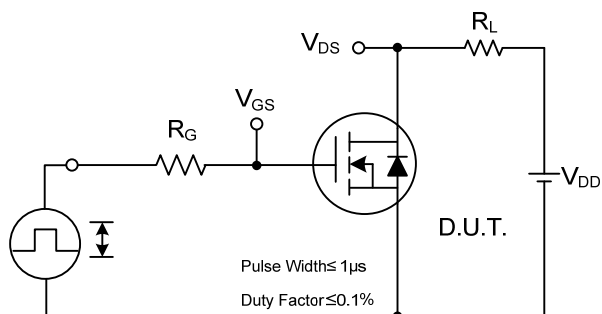


**Peak Diode Recovery  $dv/dt$  Test Circuit**

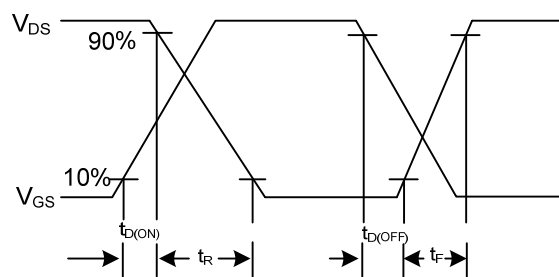


**Peak Diode Recovery  $dv/dt$  Waveforms**

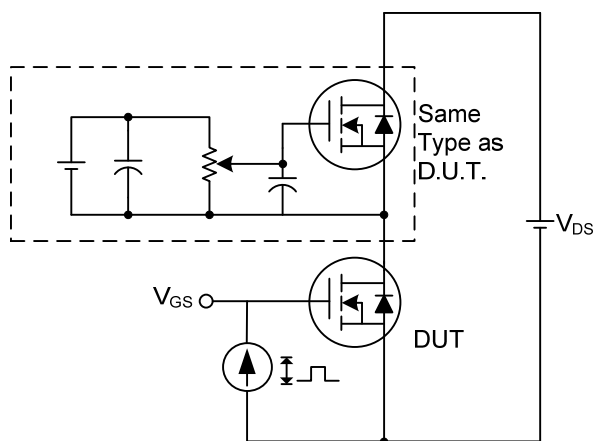
### ■ TEST CIRCUITS AND WAVEFORMS



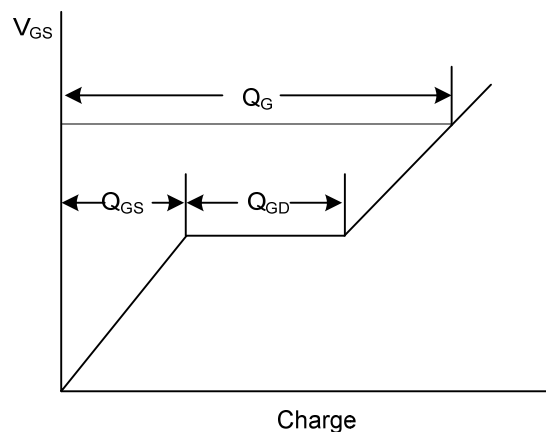
Switching Test Circuit



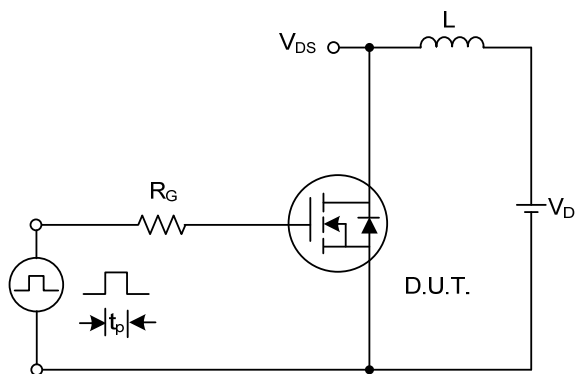
Switching Waveforms



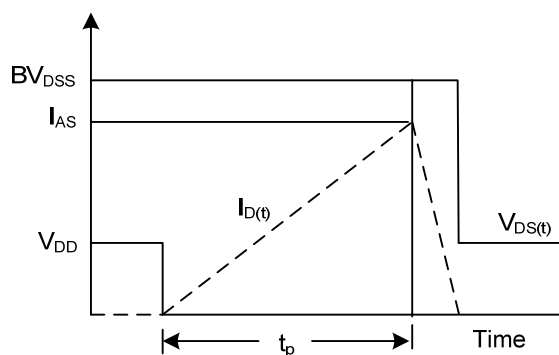
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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