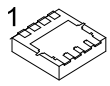
UT20N03V

Power MOSFET

20A, 30V N-CHANNEL ENHANCEMENT MODE POWER MOSFET TRANSISTOR



PDFN3×3

DFN2020-6B

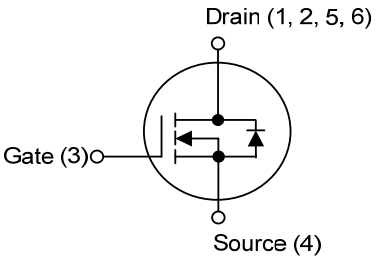
■ DESCRIPTION

The UTC **UT20N03V** is an N-channel enhancement power MOSFET using UTC's advanced technology in the various components of gate charge and capacitance have been optimized to reduce switching losses. Low gate resistance and very low Miller charge enable excellent performance with both adaptive and fixed dead time gate drive circuits. Very low RDS(ON) has been maintained to provide a sub logic-level device, designed to minimize losses in power conversion applications.

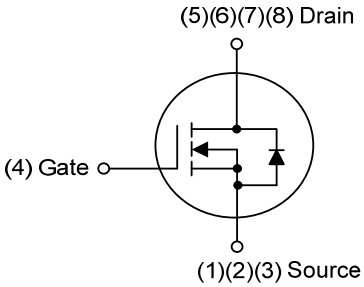
■ FEATURES

* $R_{DS(ON)}$ ≤ 11.5 mΩ @ V_{GS}=10V, I_D=20A
  $R_{DS(ON)}$ ≤ 16.5 mΩ @ V_{GS}=4.5V, I_D=10A
  $R_{DS(ON)}$ ≤ 25.5 mΩ @ V_{GS}=2.5V, I_D=7.0A
* High Switching Speed
* High Current Capacity

■ SYMBOL



DFN2020-6B



PDFN3×3

■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
UT20N03VL-P3030-R	UT20N03VG-P3030-R	PDFN3×3	S	S	S	G	D	D	D	D	Tape Reel
UT20N03VL-K06B-2020-R	UT20N03VG-K06B-2020-R	DFN2020-6B	D	D	G	S	D	D	-	-	Tape Reel

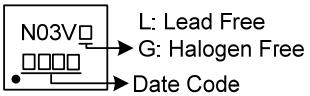
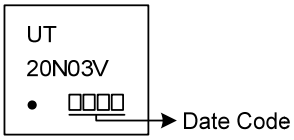
Note: Pin Assignment: G: Gate S: Source D: Drain

UT20N03VG-P3030-R

(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) P3030: PDFN3×3, K06B-2020: DFN2020-6B
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

DFN2020-6B	PDFN3×3
	

■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±12	V
Drain Current	Continuous	I_D	20	A
	Pulsed	I_{DM}	40	A
Avalanche Energy (Note 3)	Single Pulsed	E_{AS}	24.5	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2	V/ns
Power Dissipation	DFN2020-6B	P_D	10	W
	PDFN3×3		25	W
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. L = 0.1mH, I_{AS} = 9.9A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C.
4. I_{SD} ≤ 20A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	DFN2020-6B	θ_{JA}	270	°C/W
	PDFN3×3		75	°C/W
Junction to Case	DFN2020-6B	θ_{JC}	12	°C/W
	PDFN3×3		5	°C/W

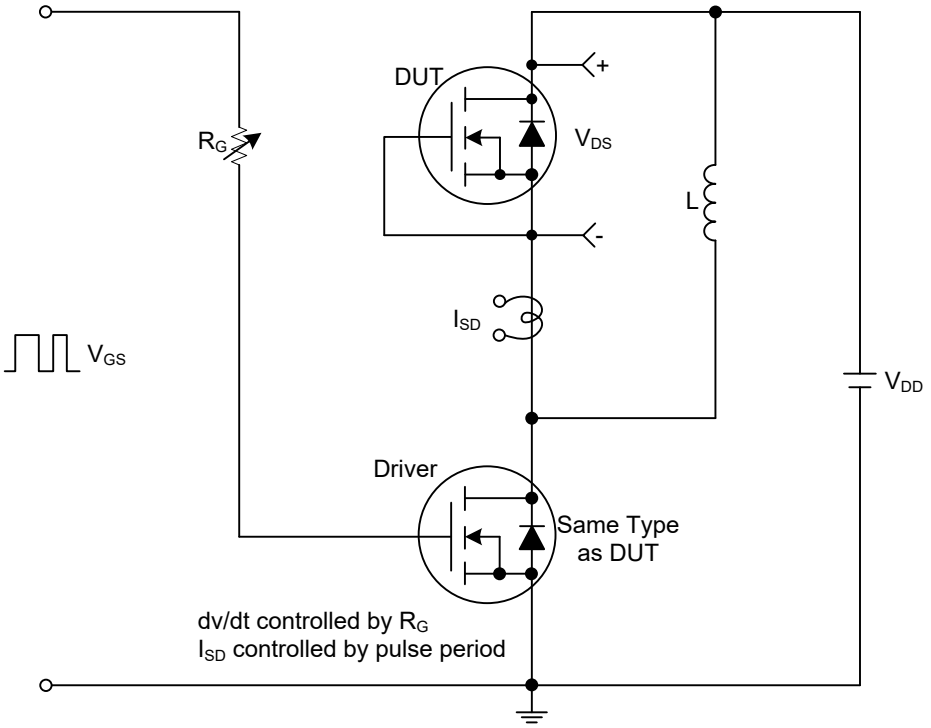
Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

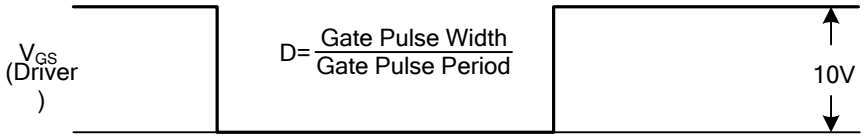
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

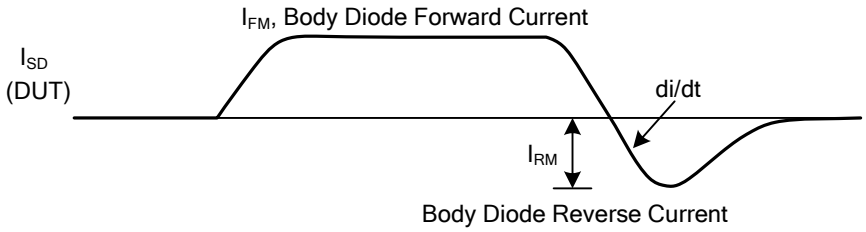
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	30			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=30V, V_{GS}=0V			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=+12V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-12V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	0.5		1.5	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=20A		9.5	11.5	mΩ
			V_{GS}=4.5V, I_D=10A		11.3	16.5	mΩ
			V_{GS}=2.5V, I_D=7.0A		18	25.5	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		972		pF
Output Capacitance		C_{OSS}			101		pF
Reverse Transfer Capacitance		C_{RSS}			88		pF
SWITCHING PARAMETERS							
Total Gate Charge		Q_G	V_{DS}=24V, V_{GS}=10V, I_D=20A (Note1, 2)		38		nC
Gate to Source Charge		Q_{GS}			3		nC
Gate to Drain Charge		Q_{GD}			8		nC
Turn-ON Delay Time		$t_{D(ON)}$	V_{DS}=15V, V_{GS}=10V, I_D=20A, R_G=3Ω (Note1, 2)		9		ns
Rise Time		t_R			18		ns
Turn-OFF Delay Time		$t_{D(OFF)}$			32		ns
Fall-Time		t_F			20		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				20	A
Maximum Body-Diode Pulsed Current		I_{SM}				40	A
Drain-Source Diode Forward Voltage		V_{SD}	I_S=1.0A, V_{GS}=0V			1.4	V
Reverse Recovery Time (Note 1)		t_{rr}	I_S=20A, V_{GS}=0V, dI/dt=100A/μs		95		ns
Reverse Recovery Charge		Q_{rr}			79		nC

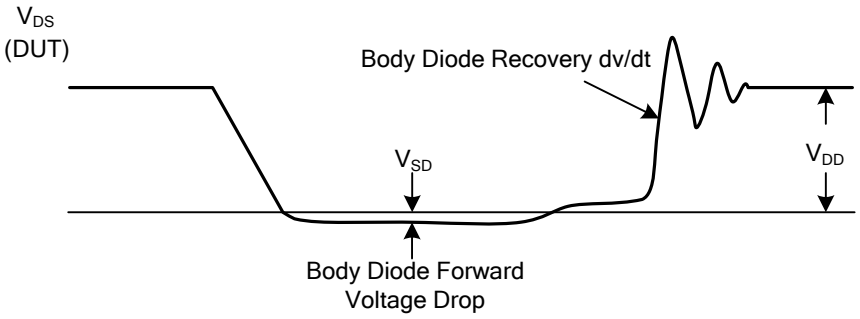
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



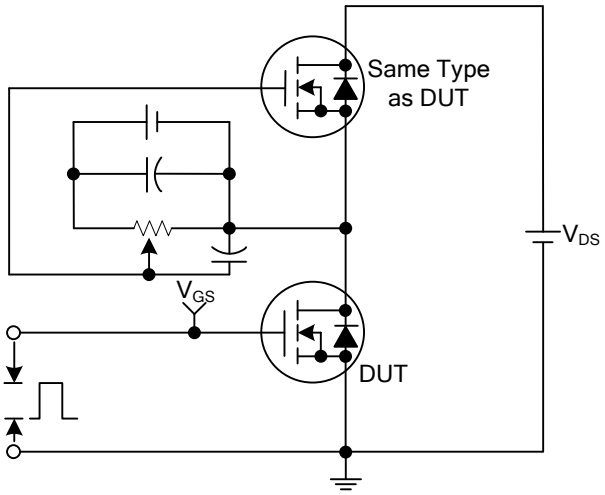




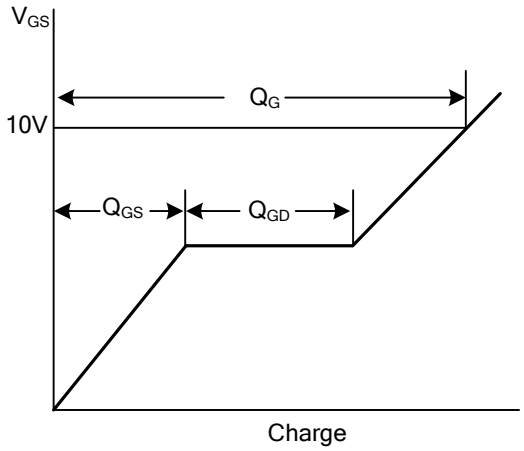


Peak Diode Recovery dv/dt Test Circuit and Waveforms

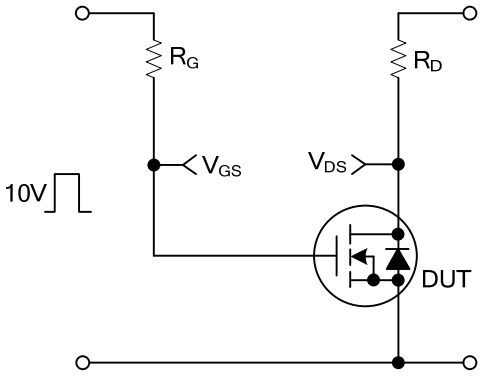
■ TEST CIRCUITS AND WAVEFORMS



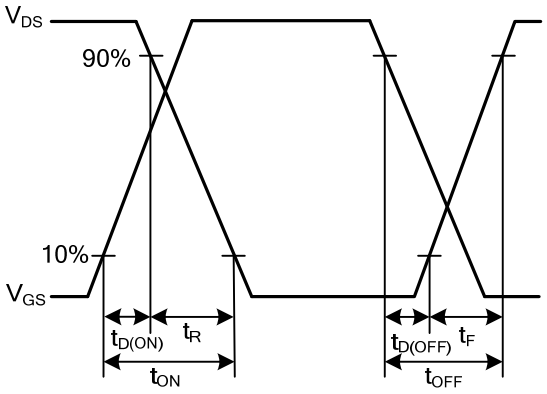
Gate Charge Test Circuit



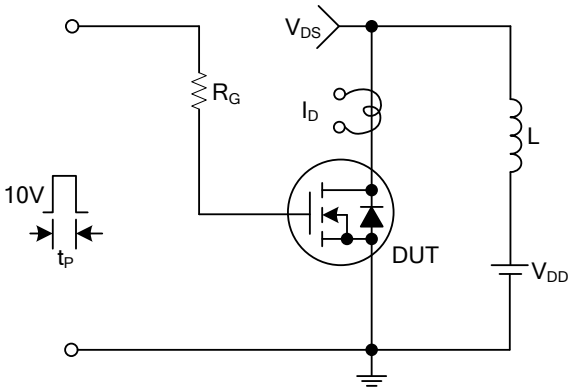
Gate Charge Waveforms



Resistive Switching Test Circuit

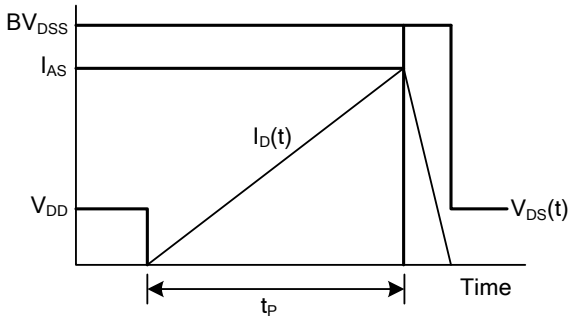


Resistive Switching Waveforms



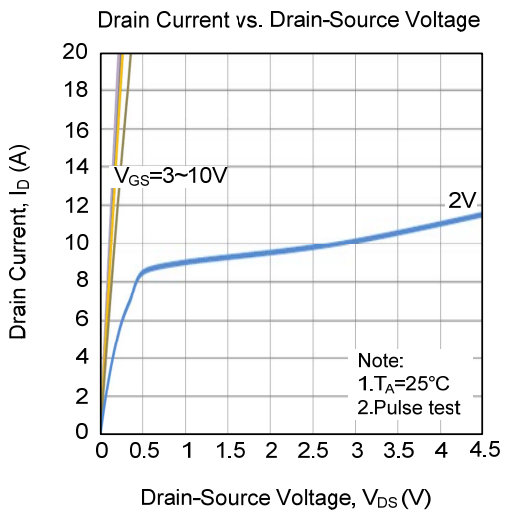
Unclamped Inductive Switching Test Circuit

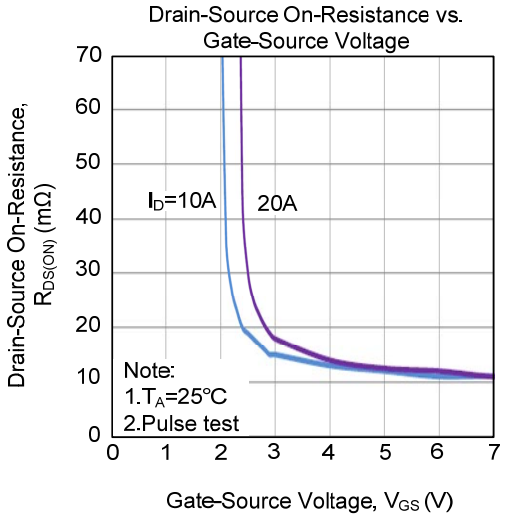
$$E_{AS}=\frac{1}{2}LI_{AS}^{2}\frac{BV_{DSS}}{BV_{DSS}-V_{DD}}$$

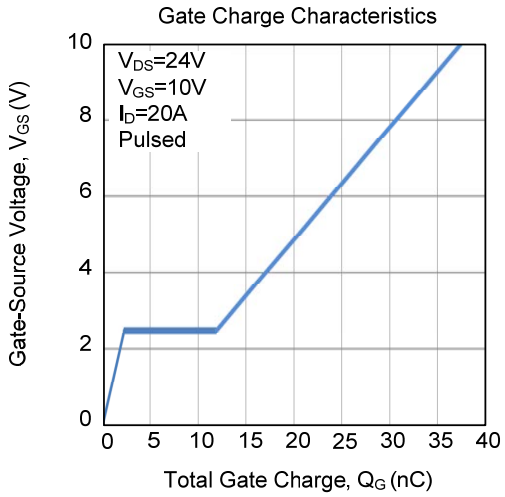


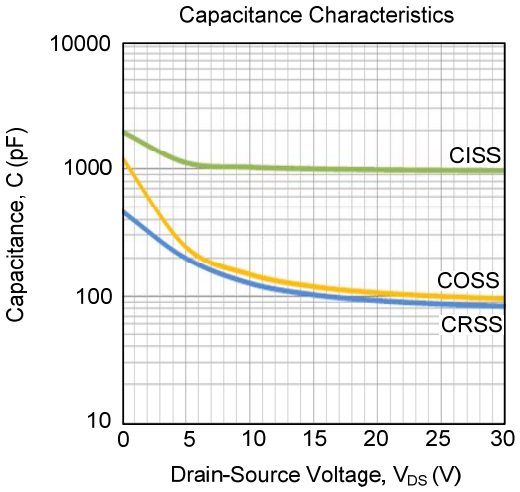
Unclamped Inductive Switching Waveforms

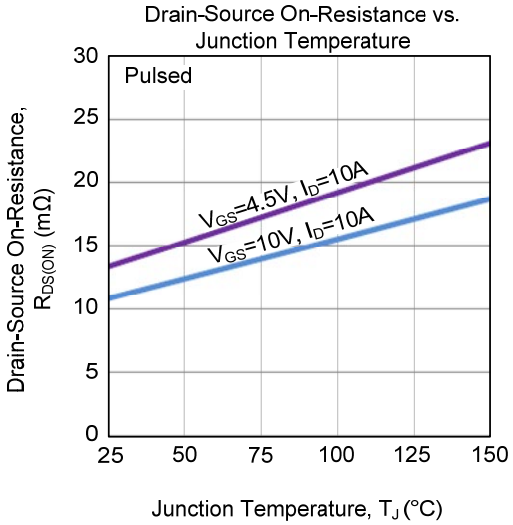
■ TYPICAL CHARACTERISTICS

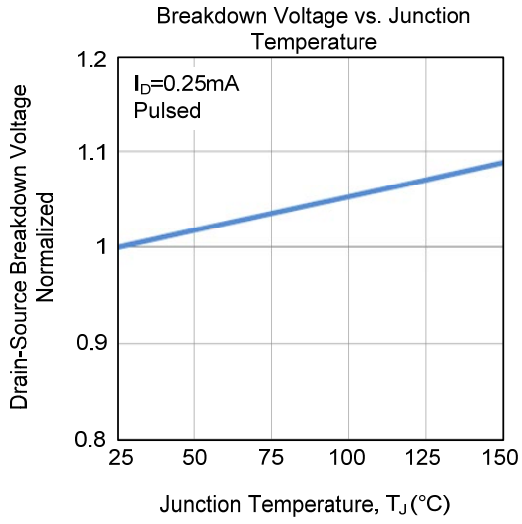






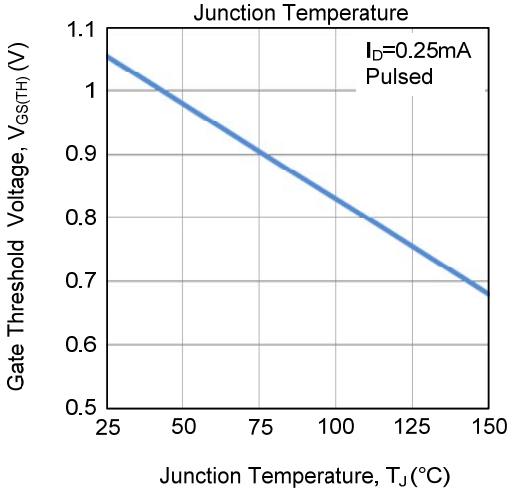




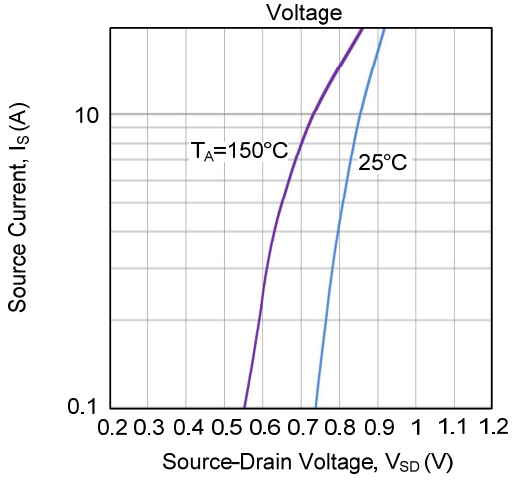


■ TYPICAL CHARACTERISTICS (Cont.)

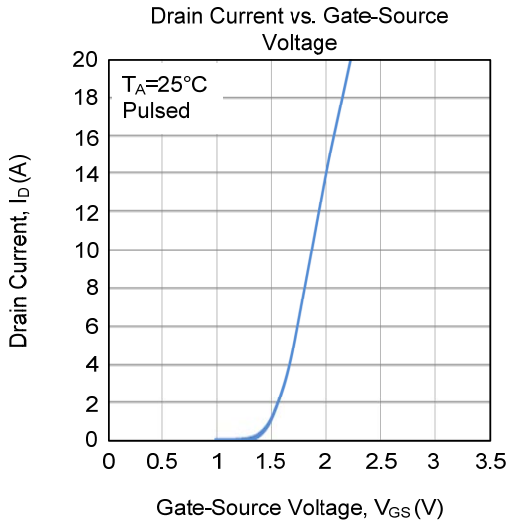
Gate Threshold Voltage vs. Junction Temperature



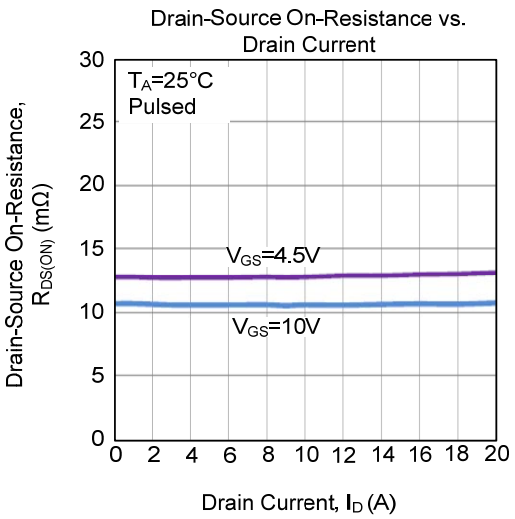
Source Current vs. Source-Drain Voltage



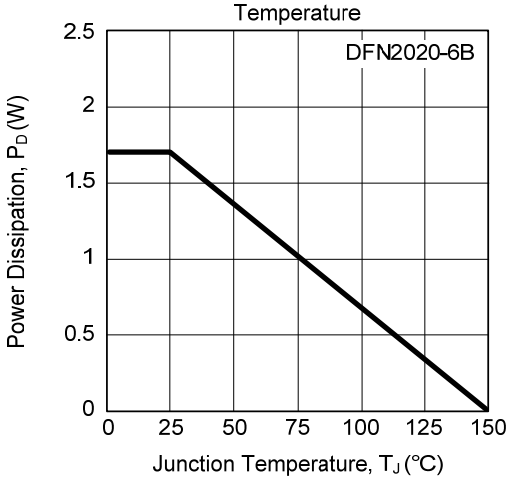
Drain Current vs. Gate-Source Voltage



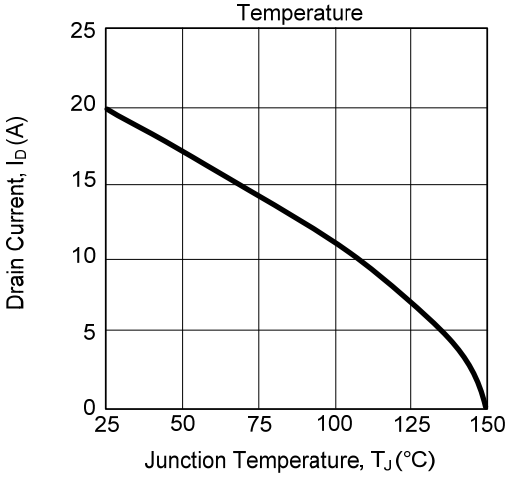
Drain-Source On-Resistance vs. Drain Current



Power Dissipation vs. Junction Temperature



Drain Current vs. Junction Temperature



■ TYPICAL CHARACTERISTICS (Cont.)