

**UT2N04LZ**

Preliminary

Power MOSFET

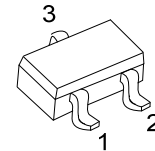
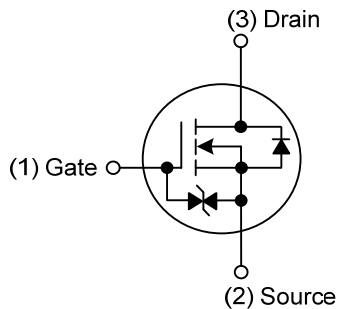
**2.0A, 40V N-CHANNEL
POWER MOSFET****DESCRIPTION**

The UTC **UT2N04LZ** employs advanced MOSFET technology and features low gate charge while maintaining low on-resistance.

Optimized for switching applications, this device improves the overall efficiency of DC/DC converters and allows operation to higher switching frequencies.

FEATURES

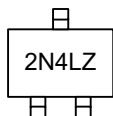
- * $R_{DS(on)} \leq 0.1 \Omega$ @ $V_{GS}=10$ $I_D=1.0A$
- * $R_{DS(on)} \leq 0.2 \Omega$ @ $V_{GS}=4.5V$, $I_D=1.0A$
- * Low Capacitance
- * Low Gate Charge
- * Fast Switching Capability
- * Avalanche Energy Specified

SYMBOL**SOT-23-3**
(JEDEC TO-236)**ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT2N04LZL-AE2-R	UT2N04LZG-AE2-R	SOT-23-3	G	S	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

UT2N04LZG-AE2-R		(1) Packing Type	(1) R: Tape Reel
		(2) Package Type	(2) AE2: SOT-23-3
		(3) Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING

■ **ABSOLUTE MAXIMUM RATINGS** ($T_C=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	Continuous	I_D	2	A
	Pulsed (Note 2)	I_{DM}	4	A
Avalanche Energy	Repetitive (Note 3)	E_{AS}	0.1	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	2.76	V/ns
Power Dissipation ($T_A=25^{\circ}\text{C}$)		P_D	0.33	W
Junction Temperature		T_J	+150	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = 1.4\text{A}$, $V_{DD} = 25\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 2.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	378	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_c board, 2oz copper, with 1inch square copper plate.

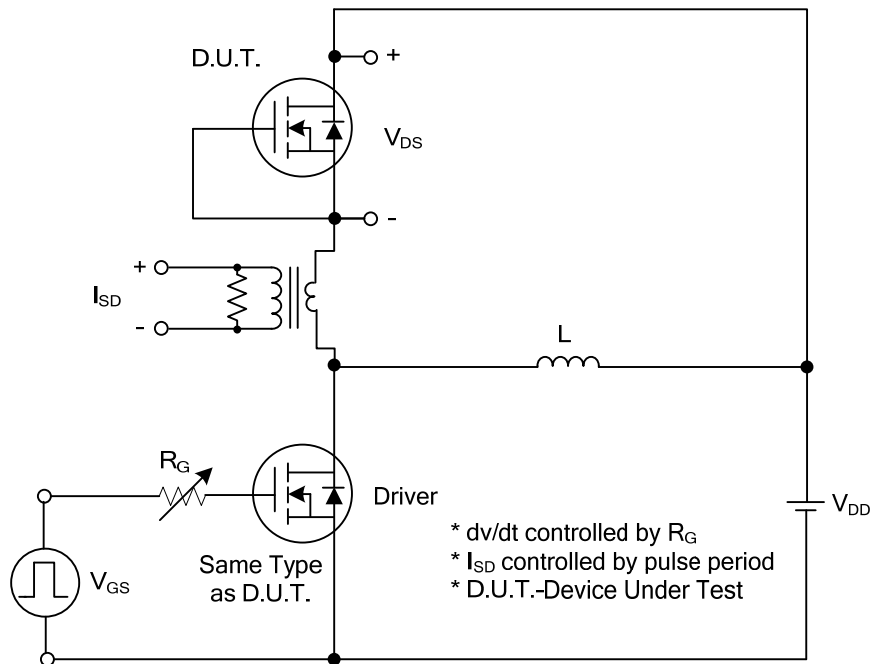
■ **ELECTRICAL CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{DS} =0V	40			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	I _{GSS}	V _{DS} =0V, V _{GS} =+20V			10	μA
	Reverse		V _{DS} =0V, V _{GS} =-20V			-10	μA
ON CHARACTERISTICS							
Gate Threshold Voltage		V _{GS(TH)}	V _{DS} = V _{GS} , I _D =250μA	0.8		2.0	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =1.0A			0.1	Ω
			V _{GS} =4.5V, I _D =1.0A			0.2	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C _{ISS}	V _{GS} =0V, V _{DS} =20V, f=1MHz		94		pF
Output Capacitance		C _{OSS}			24		pF
Reverse Transfer Capacitance		C _{RSS}			17		pF
SWITCHING PARAMETERS							
Total Gate Charge (Note 1)		Q _G	V _{DD} =32V, V _{GS} =10V, I _D =2.0A (Note 1, 2)		10		nC
Gate to Source Charge		Q _{GS}			2.1		nC
Gate to Drain Charge		Q _{GD}			2.3		nC
Turn-ON Delay Time (Note 1)		t _{D(ON)}	V _{DD} =20V, V _{GS} =10V, I _D =2.0A, R _G =3Ω (Note 1, 2)		8		ns
Rise Time		t _R			22		ns
Turn-OFF Delay Time		t _{D(OFF)}			89		ns
Fall-Time		t _F			59		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current		I _S				2	A
Maximum Pulsed Drain-Source Diode Forward Current		I _{SM}				4	A
Drain-Source Diode Forward Voltage (Note 1)		V _{SD}	I _S =2.0A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time		t _{rr}	V _{GS} = 0V, I _S =2.0A,		60		ns
Body Diode Reverse Recovery Charge		Q _{rr}	dI _F /dt=100A/μs (Note 1)		63		nC

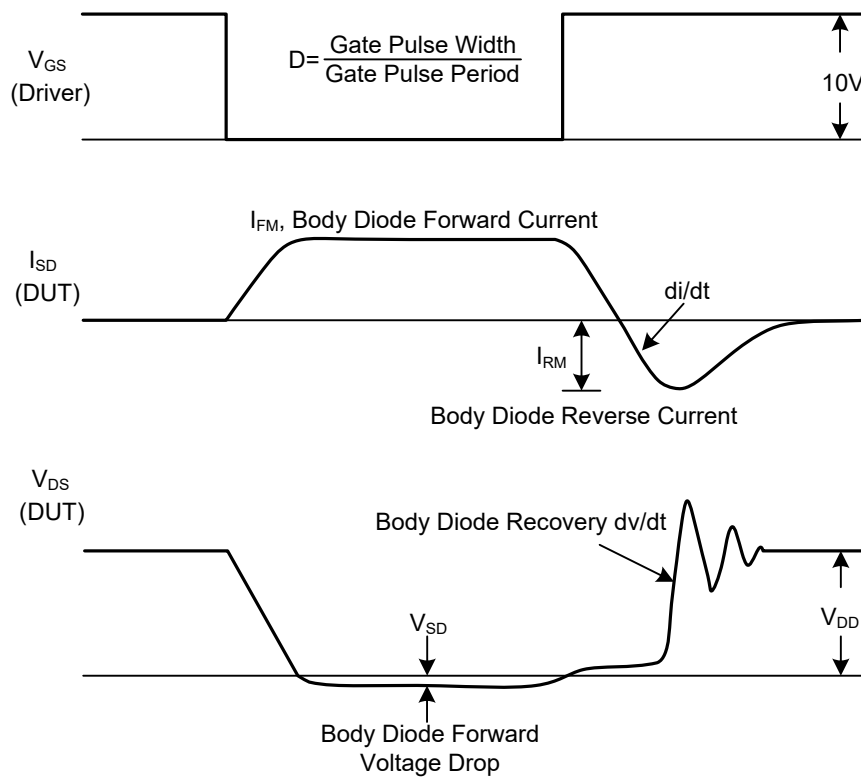
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

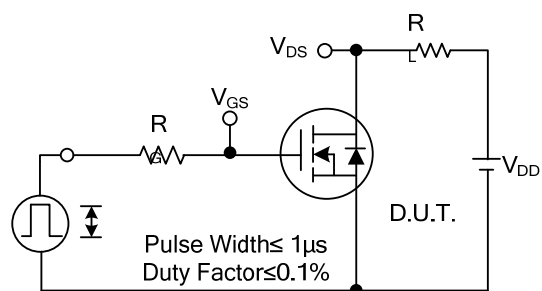


Peak Diode Recovery dv/dt Test Circuit

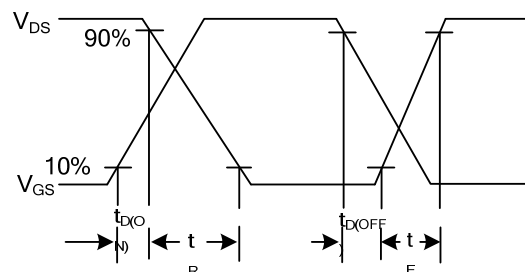


Peak Diode Recovery dv/dt Waveforms

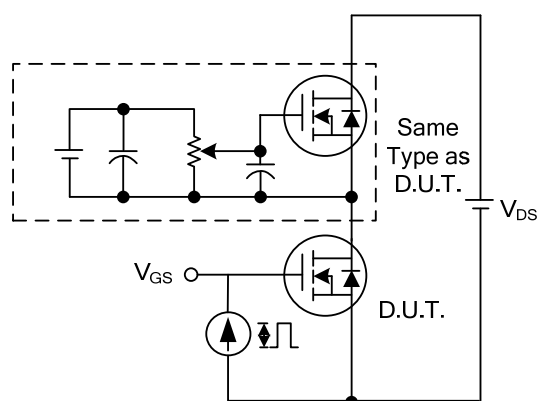
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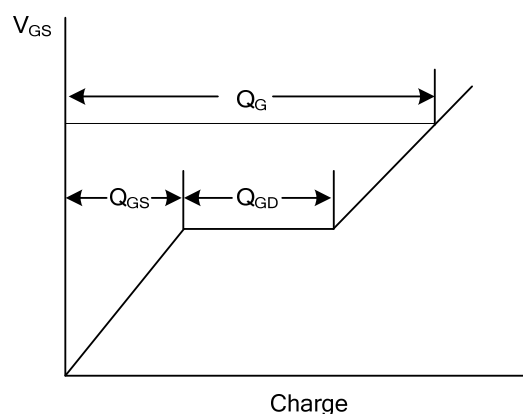
Switching Test Circuit



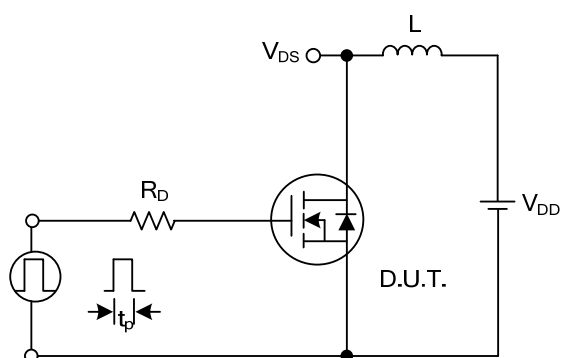
Switching Waveforms



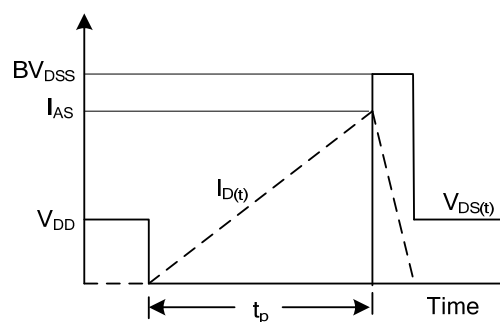
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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