

UNISONIC TECHNOLOGIES CO., LTD

UT50N03V Preliminary Power MOSFET

50A, 30V N-CHANNEL ENHANCEMENT MODE POWER MOSFET TRANSISTOR

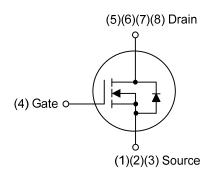
■ DESCRIPTION

The UTC **UT50N03V** is an N-channel enhancement power MOSFET using UTC's advanced technology in the various components of gate charge and capacitance have been optimized to reduce switching losses. Low gate resistance and very low Miller charge enable excellent performance with both adaptive and fixed dead time gate drive circuits. Very low RDS(ON) has been maintained to provide a sub logic-level device, designed to minimize losses in power conversion applications.



- * $R_{DS(ON)} \le 4.5 \text{ m}\Omega$ @ V_{GS} =10V, I_{D} =20A $R_{DS(ON)} \le 5.3 \text{ m}\Omega$ @ V_{GS} =4.5V, I_{D} =15A $R_{DS(ON)} \le 8 \text{ m}\Omega$ @ V_{GS} =2.5V, I_{D} =12A
- * High Switching Speed
- * High Current Capacity

■ SYMBOL



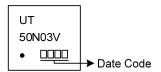
■ ORDERING INFORMATION

Ordering Number		Daalaaaa	Pin Assignment							D 1:	
Lead Free	Halogen Free	Package	1	2	3	4	5	6	7	8	Packing
UT50N03VL-P3030-R	UT50N03VL-P3030-R UT50N03VG-P3030-R		S	S	S	G	D	D	D	D	Tape Reel
Note: Pin Assignment: S: Source G: Gate D: Drain											
UT50N03VG- <u>P3030-R</u>											
	(1) R: Tape Reel										
	(2) P3030: PDFN3×3										
	(3) G: Halogen Free and Lead Free, L: Lead Free										

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MARKING



■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V _{GSS}	±12	V
Drain Current	Continuous	l _D	50	Α
	Pulsed	I _{DM}	100	Α
Avalanche Energy (Note 3)	Single Pulsed	Eas	51	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.5	V/ns
Power Dissipation		PD	34	W
Junction Temperature		TJ	150	°C
Storage Temperature		T _{STG}	-55 ~ 150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- 2. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 3. L=0.1mH, I_{AS}=32A, V_{DD} =20V, R_{G} =25 Ω , Starting T_{J} = 25 $^{\circ}$ C
- 4. $I_{SD} \le 30A$, $di/dt \le 200A/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25$ °C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θја	75	°C/W
Junction to Case	θις	3.67	°C/W

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

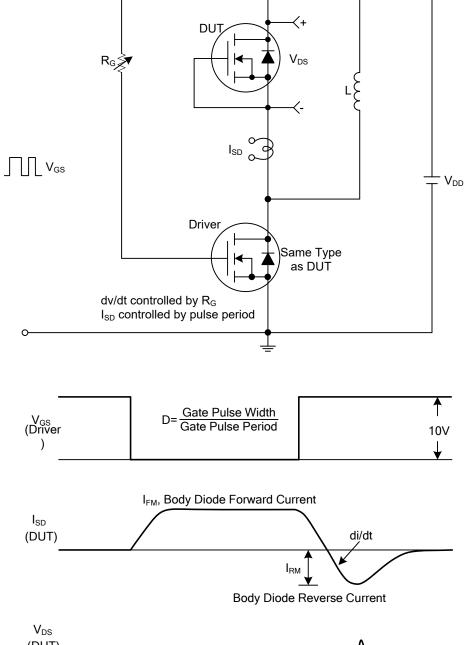
■ ELECTRICAL CHARACTERISTICS (T」=25°C, unless otherwise specified)

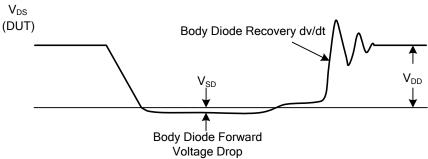
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS		_					
Drain-Source Breakdown Voltage		BV _{DSS}	I _D =250μA, V _{GS} =0V	30			V
Drain-Source Leakage Current		I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μΑ
Gate- Source Leakage Current	Forward	Lana	V _{GS} =+12V, V _{DS} =0V			+100	nA
	Reverse	Igss	V _{GS} =-12V, V _{DS} =0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V _{DS} =V _{GS} , I _D =250μA	0.5		1.5	V
Static Drain-Source On-State Resistance		R _{DS(ON)}	V _{GS} =10V, I _D =20A			4.5	mΩ
			V _{GS} =4.5V, I _D =15A			5.3	mΩ
			V _{GS} =2.5V, I _D =12A			8.0	mΩ
DYNAMIC PARAMETERS							
Input Capacitance		Ciss			3330		pF
Output Capacitance		Coss	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		330		pF
Reverse Transfer Capacitance		Crss			300		pF
SWITCHING PARAMETERS							
Total Gate Charge		\mathbf{Q}_{G}	\ -24\\ \ \ -4.5\\ -50A		65		nC
Gate to Source Charge		Q _G s	V _{DS} =24V, V _{GS} =4.5V, I _D =50A (Note1, 2)		8.5		nC
Gate to Drain Charge		Q_{GD}	(Note 1, 2)		24		nC
Turn-ON Delay Time		$t_{D(ON)}$			9		ns
Rise Time		t_{R}	V _{DS} =15V, V _{GS} =10V, I _D =50A,		20		ns
Turn-OFF Delay Time		t _{D(OFF)}	R _G =3.3Ω (Note1, 2)		80		ns
Fall-Time		t⊦			28		ns
SOURCE- DRAIN DIODE RATIN	IGS AND C	CHARACTERI	STICS				
Maximum Body-Diode Continuous Current		Is				50	Α
Maximum Body-Diode Pulsed Cu	ırrent	lsм				100	Α
Drain-Source Diode Forward Volt	tage	V _{SD}	I _S =50A, V _{GS} =0V			1.5	V
Reverse Recovery Time (Note 1)		trr	I _S =30A, V _{GS} =0V,		90		ns
Reverse Recovery Charge		Qrr	dI/dt=100A/μs 80				nC

Notes: 1. Pulse Test: Pulse width \leq 300 μ s, Duty cycle \leq 2%.

^{2.} Essentially independent of operating temperature.

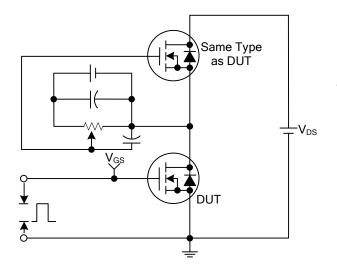
■ TEST CIRCUITS AND WAVEFORMS

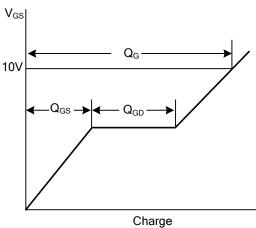




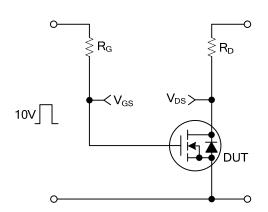
Peak Diode Recovery dv/dt Test Circuit and Waveforms

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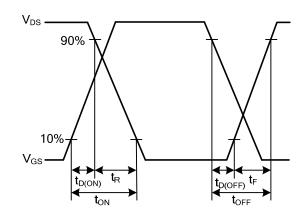




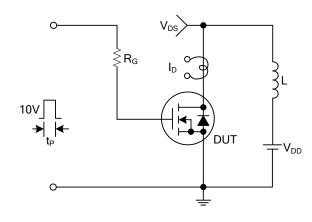
Gate Charge Test Circuit



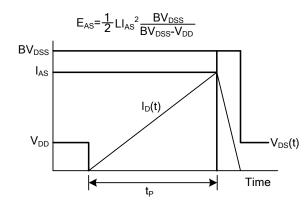
Gate Charge Waveforms



Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit

Unclamped Inductive Switching Waveforms

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